

RESEARCH ARTICLE

Stateful Logic Using Selector-Only-Memory With Tunable Operation Directionality

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ABSTRACT

The growing demand for energy- and area-efficient computing in edge devices has highlighted the limitations of conventional von Neumann architectures, which suffer from the memory bottleneck due to frequent data transfer between logic and memory units. Processing-in-memory (PIM) has emerged as a promising solution, and among its approaches, stateful logic enables computation directly within memory arrays using simple voltage pulses. To realize this concept, we demonstrate the stateful logic functionality using selector-only-memory (SOM) device based on Sn-doped GeSeTe (SGST). The device reveals a distinctive switching behavior, where the direction of threshold switching can be reversibly tuned by adjusting the external series resistance. This behavior originates from RC delay effects, which induce a residual opposite-polarity voltage during the falling edge of the input pulse. Utilizing this property, we implement various stateful logic operations—including IMPLY, NAND, NOR, AND, and OR—directly within the SOM array. Furthermore, a half-adder circuit is experimentally realized, confirming the scalability of the approach. The low off-state current and reconfigurable switching behavior make the SOM device highly suitable for dense and low-power logic-in-memory architectures, particularly in large-scale arrays for edge computing. This work will provide a new direction for designing stateful logic devices with both structural simplicity and functional versatility.

1 | Introduction

The rapid proliferation of edge devices—such as those used in IoT systems, wearable electronics, and autonomous sensing—has led to increasing demand for computing architectures capable of efficient data processing under strict power and area constraints [1–4]. In such environments, the physical separation between processing units and memory units imposes significant limitations on performance and energy efficiency due to the overhead of frequent data movement. The conventional von Neumann architecture, which inherently suffers from the memory bottleneck, is fundamentally inadequate for overcoming these

limitations. As a result, processing-in-memory (PIM) technology has gained attention as a promising alternative. By enabling computation and storage within the same physical location, PIM significantly reduces data movement, power consumption, and response latency [5–8]. These characteristics make it a highly suitable approach for implementing high-efficiency, high-density computing systems in edge applications.

The selector-only-memory (SOM), which integrates both selection and storage functionalities within a single device, has recently gained attention as a promising candidate for implementing PIM architecture. SOM devices are typically based on

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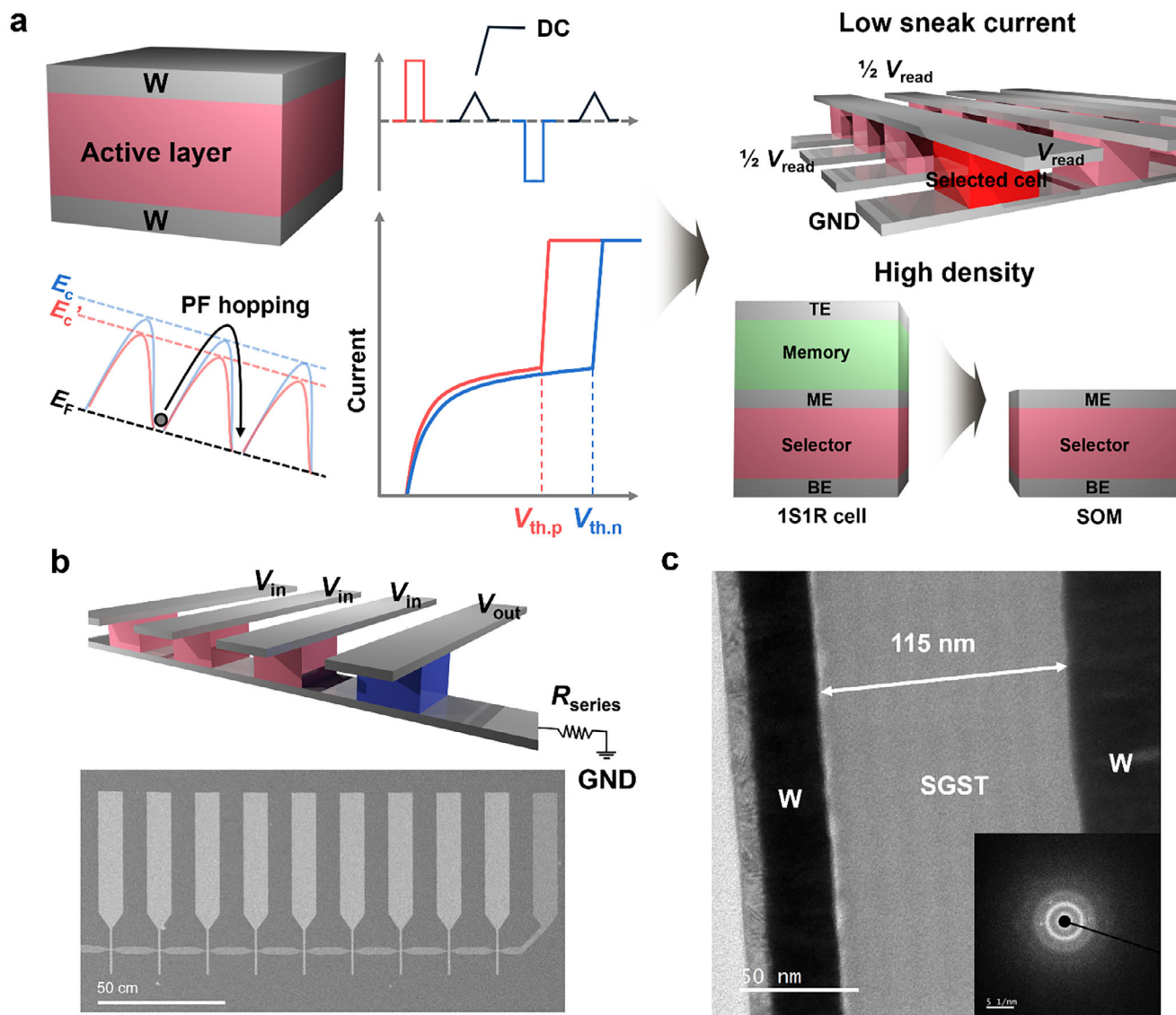


FIGURE 1 | (a) Schematic illustration and electrical characteristics of the SOM device consisting of a W/active layer/W structure and the I-V curve exhibits bidirectional threshold switching with different positive and negative threshold voltages ($V_{th,p}$ and $V_{th,n}$). In the off-state region, conduction is governed by trap-assisted PF hopping through a large density of localized trap states within the chalcogenide layer. The device enables high-density integration and suppressing sneak currents in crossbar arrays. (b) Three-dimensional schematic of stateful logic and SEM image of fabricated crossbar array structures. (c) Cross-sectional HR-TEM image of the SOM device, showing a 115 nm thick SGST (SnGeSeTe) layer sandwiched between W electrodes. The inset shows the selected area diffraction pattern (SADP), confirming the amorphous phase of the SGST layer.

ovonic threshold switches (OTS), exhibiting high nonlinearity, abrupt threshold switching behavior, and extremely low off-state current [9–13]. As shown in Figure 1a, SOM exhibits a polarity-dependent, nonvolatile modulation of the threshold voltage (V_{th}), determined by the polarity of previously applied voltage pulses. This behavior has been attributed to the presence of numerous trap states in the chalcogenide-based intermediate layer, which may cause modulation of the Poole–Frenkel (PF) conduction barrier depending on pulse polarity [14, 15]. As a result, V_{th} becomes electrically tunable, enabling its effective use for storing and controlling logical states. In addition, compared to conventional memory devices such as resistive random access memory (RRAM) and phase-change random access memory (PCRAM), SOMs demonstrate superior structural and electrical advantages, including low sneak current even in large-scale arrays and

simplified cell structures that allow for high integration density without requiring additional selectors [9, 16, 17].

To implement PIM architectures that perform data storage and processing in the same physical location, stateful logic has been proposed as an effective approach. In stateful logic, logical states are stored directly in memory cells, and logic operations are performed by applying voltages between cells, thereby blurring the boundary between computation and storage. This architecture enables direct logic operations within memory arrays without separate logic circuits, offering advantages such as (structural simplicity, improved energy efficiency, and ease of parallel processing [18–22]. As illustrated in Figure 1b, logic operations are implemented by applying input voltages (V_{in}) to the designated input cells (red-colored cells) and an output voltage (V_{out}) to

the target output cell (blue-colored cell), with a series resistor connected to the common ground. Applying V_{out} to the output cell programs its state in accordance with the intended logic function. In this work, we fabricated a SOM-based array structure and verified its physical configuration using scanning electron microscope (SEM) imaging. Earlier demonstrations of stateful logic were based on memristor devices implementing IMPLY operations and have since been extended to various logic gates using nonvolatile memory (NVM) devices such as RRAM and PCRAM [18–20]. However, these NVM-based approaches suffer from high off-state current and sneak-path-induced malfunction. These limitations become more pronounced in large-scale memory arrays, posing significant challenges to practical implementation and scalability. In particular, RRAM and PCRAM devices inherently require integration of a dedicated selector in series with each memory cell to suppress leakage currents, which further increases fabrication complexity and limits array density [23–26].

In this study, we investigated the switching behavior of SOM-based array structures and observed that the directionality of V_{th} -switching can be reversibly modulated by varying the external series resistance within the same device structure [27, 28]. This directionality control allows multiple stateful logic functions to be selectively realized within a single SOM platform without modifying the device structure. These features demonstrate the potential of SOM as a memory element as well as a reconfigurable logic device with intrinsic switching versatility. The SOM device used in this work employed a Sn-doped GeSeTe (SGST) chalcogenide compound as the active layer. The atomic composition of the SGST layer was confirmed by Auger electron spectroscopy (AES) analysis and determined to be Sn:Ge:Se:Te = 7.0:23.0:29.7:40.3, as shown in Figure S1. SGST was selected because it exhibits stable threshold-switching behavior and a sufficiently wide memory window, enabling reliable state discrimination during stateful logic operations [29]. As shown in Figure 1c, cross-sectional transmission electron microscopy (TEM) and selected-area electron diffraction (SAED) analyses confirm that the SGST layer is in the amorphous phase [30–32]. A 115 nm-thick SGST layer was selected to provide stable threshold-switching characteristics and suppress leakage current during the stateful logic demonstrations presented in this work.

Based on the characteristics above, various binary logic operations were experimentally demonstrated using the SOM device, including IMPLY, NAND, NOR, AND, and OR gates. These operations were implemented without the need for complex peripheral circuits, relying solely on the application of simple voltage pulses, thereby confirming the practical feasibility of SOM-based stateful logic. Furthermore, by combining these basic operations, a half-adder circuit was constructed and experimentally verified, suggesting that SOM devices are capable of implementing not only elementary logic gates but also more complex logic functions. In particular, the extremely low off-state current of the SOM enables reliable logic operations in large-scale arrays without malfunction due to sneak current. In addition, the ability to control the V_{th} -switching directions through external series resistance allows for directionally reconfigurable logic operations within the same cell structure.

2 | Result and Discussion

2.1 | Switching Polarity Modulation Via Series Resistance Control

Figure 2a illustrates the schematic of the measurement circuit used to characterize the SOM devices. An arbitrary function generator (AFG) was used to apply voltage pulses to the device, and an oscilloscope (OSC) with an internal resistance of 1 M Ω was employed to measure the voltages across both the series resistor (R_{series}) and the SOM. By connecting the series resistor in line with the SOM, the circuit allowed simultaneous monitoring of the device voltage and current. All unit-cell pulse measurements were performed using this configuration.

Figure 2b presents a transient measurement obtained with a 4 k Ω series resistor when a 1 μ s pulse width, 5 V amplitude voltage pulse was applied. The traces show the input voltage (V_{in} , black-colored line), the voltage across the resistor (V_{R} , red-colored line), and the voltage across the SOM (V_{SOM} , green-colored line). Since $V_{\text{in}} = V_{\text{R}} + V_{\text{SOM}}$, both V_{R} and V_{SOM} exhibit positive amplitudes during the pulse, generating a positive electric field across the SOM. At the beginning of the pulse, the parasitic capacitance originating from the device and measurement setup (including probe pads, wiring, and the device structure), together with the series resistor, induces an RC delay that governs the initial voltage dynamics across the SOM. This causes V_{R} to increase exponentially, while V_{SOM} gradually decreases as the device switches from high to low resistance. After the pulse terminates, V_{in} drops to 0 V; however, due to the resistive and capacitive components of both the resistor and the SOM, an RC delay occurs, producing a transient decay in V_{R} . This decay drives a momentary negative voltage across the SOM, resulting in a transient negative electric field, as indicated by the post-pulse waveform. This phenomenon can affect the logical state of the SOM, which exhibits bias-polarity-dependent V_{th} -switching. Furthermore, the intensity of the post-pulse waveform is controlled by the magnitude of the series resistor (RC delay), and the directionality of V_{th} -switching can be modulated.

To quantify this effect, the minimum negative voltage across the SOM was defined as V_{min} , and the decay time constant τ was defined as the time required for V_{SOM} to decrease from V_{min} to 37% of its minimum value [33, 34]. As shown in Figure 2c, both $|V_{\text{min}}|$ and τ become larger as the series resistance increases. The voltage–time integral of the residual opposite-polarity pulse was additionally analyzed, as shown in Figure S2, to quantify the cumulative effect of the RC-delay-induced transient pulse. Since SOM devices are known to exhibit nonvolatile modulation of the V_{th} depending on the polarity of the previously applied pulse, an increase in the magnitude and duration of this negative electric field can significantly affect V_{th} [35, 36].

Figure 2d shows the variation of V_{th} as a function of the series resistance value. Here, $V_{\text{th,p}}$ (red-colored) denotes the V_{th} measured after applying a positive pulse, while $V_{\text{th,n}}$ (blue-colored) represents the value after a negative pulse, as indicated by the pulse scheme in the inset of Figure 2d. A detailed description of the read-pulse measurement protocol is provided in Figure S3. With increasing series resistance, $V_{\text{th,p}}$ increases, whereas

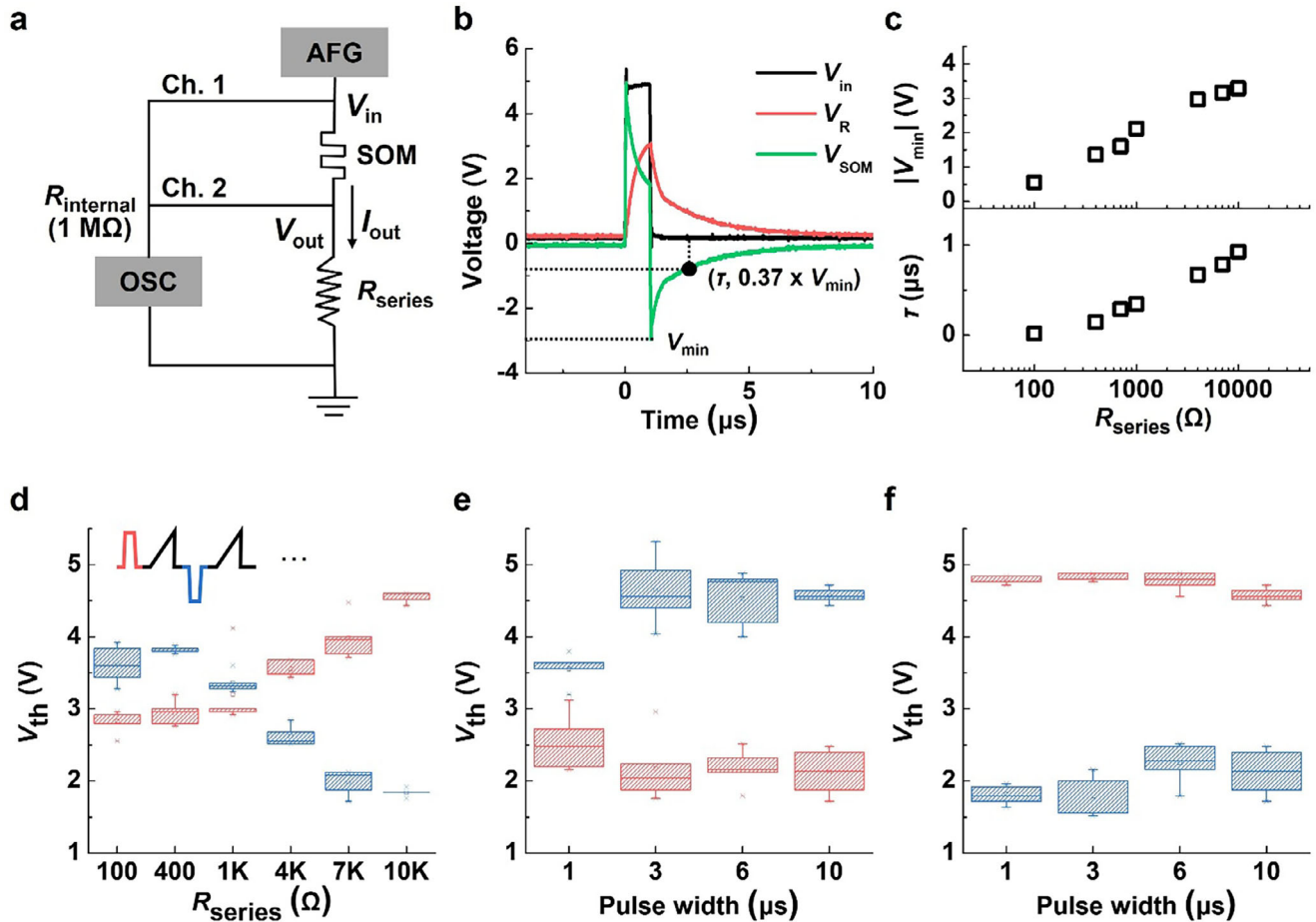


FIGURE 2 | (a) Schematic measurement setup for threshold switching characteristics of the SOM device, consisting of an AFG, OSC, and series resistance (R_{series}). (b) Transient voltage response of the SOM device under a 1 μs programming pulse with an external series resistance of 4 kΩ. The applied input (V_{in}), node voltage (V_{R}), and device voltage (V_{SOM}) are shown, illustrating the undershoot (V_{min}) and relaxation time constant (τ) arising from RC delay effects. (c) Extracted values of $|V_{\text{min}}|$ and τ as a function of R_{series} , indicating that both parameters increase with larger R_{series} . (d) Dependence of threshold voltages by positive (red) and negative (blue) write pulse on R_{series} . (e) Dependence of threshold voltages by positive and negative write pulse on pulse width in 400 Ω. (f) Dependence of threshold voltages by positive and negative write pulse on pulse width in 10 kΩ.

$V_{\text{th,n}}$ decreases. This behavior indicates that a larger resistance prolongs and enhances the negative electric field generated after a positive pulse (and vice versa), driving $V_{\text{th,p}}$ toward $V_{\text{th,n}}$ and $V_{\text{th,n}}$ toward $V_{\text{th,p}}$. As a result, the relative magnitude relationship between $V_{\text{th,p}}$ and $V_{\text{th,n}}$ changes, such that the initially lower V_{th} becomes higher than the other between 1 and 4 kΩ, offering a controllable means to reverse the V_{th} -switching polarity without altering the device structure.

To further analyze this polarity reversal behavior, two representative resistance values were selected: 400 Ω, where $V_{\text{th,p}} < V_{\text{th,n}}$, and 10 kΩ, where $V_{\text{th,p}} > V_{\text{th,n}}$. Figure 2e shows that with 400 Ω, increasing the write-pulse width reduces $V_{\text{th,p}}$ while increasing $V_{\text{th,n}}$, thereby widening the memory window (difference between $V_{\text{th,n}}$ and $V_{\text{th,p}}$, MW). In contrast, Figure 2f demonstrates that with 10 kΩ, $V_{\text{th,n}}$ increases and $V_{\text{th,p}}$ decreases, resulting in a narrowing of the memory window. These findings confirm that the switching directionality in SOM devices can be effectively tuned via the series resistance, enabling polarity control of the V_{th} modulation. Based on these polarity-tuning results, subsequent electrical characterization and reliability evaluations were carried out using a 3 μs write pulse for the 400 Ω configuration and a 1

μs write pulse for the 10 kΩ configuration. Although the intrinsic threshold-switching speed is below 50 ns, as shown in Figure S4, longer pulse widths were employed in the logic demonstrations to ensure stable logic operation and sufficient threshold-voltage separation between logic states. To further verify the reversibility of the resistance-controlled threshold modulation, the series resistance was repeatedly alternated between 400 and 10 kΩ. As shown in Figure S5, stable threshold modulation was maintained throughout the repeated resistance-switching cycles, confirming the reversible nature of the proposed operation.

Figure 3 compares the electrical characteristics and reliability of SOM devices for two representative series resistance values: 400 and 10 kΩ. Figure 3a–c presents the DC and AC current–voltage (I–V) results for $R_{\text{series}} = 400 \Omega$. In the DC I–V characteristics shown in Figure 3a, $V_{\text{th,p}} = 1.7 \text{ V}$ and $V_{\text{th,n}} = 4.1 \text{ V}$ were observed, corresponding to a MW of 2.4 V. The V_{th} switching behavior, monitored over 50 consecutive cycles using a single triangular read pulse as presented in Figure 3b, shows stable alternation between the two V_{th} states. The cumulative distributions in Figure 3c reveal that $V_{\text{th,p}}$ has a mean of 2.1 V ($\sigma = 0.30$) and $V_{\text{th,n}}$ has a mean of 4.6 V ($\sigma = 0.23$), with the smallest observed

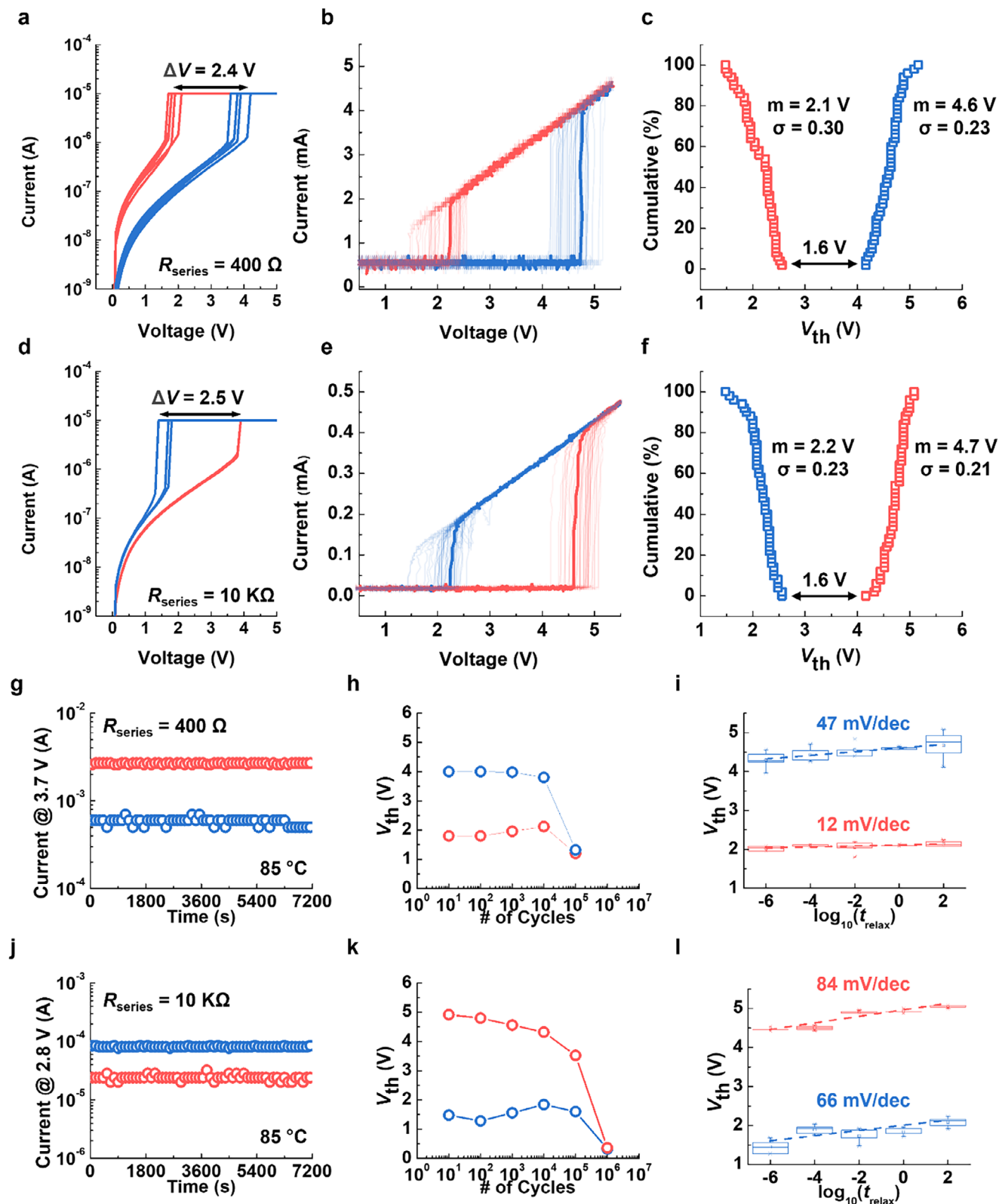


FIGURE 3 | Electrical performance of SOM devices under different series resistances. (a) DC I-V switching characteristics with $R_{\text{series}} = 400 \, \Omega$. (b) Pulsed switching results over 50 cycles with the same resistance configuration. (c) Cumulative threshold voltage distributions extracted from the 50-cycle pulsed switching measurements in (b), together with extracted mean (m) and standard deviation (σ). (d) DC I-V switching for $R_{\text{series}} = 10 \, \text{k}\Omega$. (e) Pulsed switching operation over 50 cycles. (f) Threshold voltage distributions for the $10 \, \text{k}\Omega$ case. (g) Retention test at 85°C with a read bias of $2.8 \, \text{V}$ for $R_{\text{series}} = 400 \, \Omega$. (h) Endurance characteristics for the $400 \, \Omega$ configuration. (i) V_{th} drift characteristics for the $400 \, \Omega$ case. (j) Retention test for $R_{\text{series}} = 10 \, \text{k}\Omega$. (k) Endurance for the $10 \, \text{k}\Omega$ case. (l) V_{th} drift characteristics under $10 \, \text{k}\Omega$ series resistance.

separation between the two states being 1.6 V, demonstrating clear bistability.

For the case of $R_{\text{series}} = 10 \text{ k}\Omega$, the DC characteristics shown in Figure 3d yield $V_{\text{th},n} = 1.3 \text{ V}$ and $V_{\text{th},p} = 3.8 \text{ V}$, corresponding to a MW of 2.5 V. When the V_{th} switching behavior was monitored over 50 consecutive cycles using AC read measurements, as presented in Figure 3e, the two states remained distinct and stable. The cumulative distributions in Figure 3f indicate that $V_{\text{th},n}$ has a mean of 2.2 V ($\sigma = 0.23$) and $V_{\text{th},p}$ has a mean of 4.7 V ($\sigma = 0.21$), with a minimum observed separation of 1.6 V. Comparing the two configurations (400 and 10 k Ω), the V_{th} states are consistently well-separated, but their relative magnitudes are inverted depending on the series resistance value. To further investigate the threshold-voltage modulation behavior, additional PF fitting results obtained under the representative resistance conditions of 400 and 10 k Ω are provided in Figure S6.

Figure 3g–i illustrates the reliability performance of the SOM devices under both series resistance conditions. In the retention measurements at 85 °C, shown in Figure 3g and 3j, both configurations maintained their V_{th} states for more than 2 hour, demonstrating robust nonvolatile behavior. For the sake of convenience, the V_{th} state of each case was verified by current responses at the given read voltage (the mean of $V_{\text{th},p}$ and $V_{\text{th},n}$). Endurance testing, presented in Figure 3h and 3k, revealed that the 400 Ω configuration supported stable switching up to 10^4 cycles, whereas the 10 k Ω configuration extended endurance to 10^5 cycles before the MW collapsed. This difference in endurance is attributed to the higher current flowing in the low-resistance state for the 400 Ω configuration, which increases the energy dissipated during switching. Such excess energy accelerates local structural changes, including trap redistribution and atomic rearrangements, ultimately leading to earlier device failure.

The V_{th} drift characteristics, which represent the amount of V_{th} variability during the time interval between writing and reading (as shown in Figures 3i and 3l), indicate that for a series resistance of 400 Ω , $V_{\text{th},n}$ and $V_{\text{th},p}$ drift at rates of 47 mV/dec and 12 mV/dec, respectively, whereas for 10 k Ω , the corresponding drift rates increase to 66 and 84 mV/dec. This drift arises from gradual relaxation processes occurring in the chalcogenide layer after programming, including redistribution of trap states and local bond rearrangements [37, 38]. Such processes are influenced by the transient electric fields applied during and immediately after the switching event. The results suggest that, while both resistance configurations maintain performance adequate for stateful logic, variations in series resistance may affect the stability of switching and the magnitude of drift through its impact on post-switching relaxation dynamics. Additional device-to-device (D2D) statistical characterization, including pulse I–V, endurance, and threshold-voltage drift measurements obtained from multiple SOM cells, is provided in Figure S7–S9 to further verify the reproducibility of the SOM operation.

2.2 | Implementation of Logic Operations in SOM-Based Stateful Logic

Based on the observations that the polarity relationship between $V_{\text{th},p}$ and $V_{\text{th},n}$ can be reversed by adjusting the series resistance,

this property was incorporated into the logic operation design. To clarify how this tunable polarity affects the device response during logic execution, we first analyzed the switching characteristics of the SOM under positive write pulse application, as shown in Figures S10a and S10b. In this study, we defined the application of a positive pulse as the write operation, which serves as the fundamental basis for subsequent logic execution.

Here, the logic states are defined according to the relative V_{th} of the SOM device: the high-threshold state is designated as logic “0”, whereas the low-threshold state is designated as logic “1.” When a positive write pulse is applied, two distinct responses emerge depending on the relative magnitudes of $V_{\text{th},p}$ and $V_{\text{th},n}$. If $V_{\text{th},p} < V_{\text{th},n}$ and the device is initially set to logic “0”, the application of a positive pulse decreases the effective V_{th} , thereby shifting the device into the logic “1” state. Conversely, when $V_{\text{th},n} < V_{\text{th},p}$ and the device is initially set to logic “1”, a positive write pulse shifts V_{th} from $V_{\text{th},n}$ toward $V_{\text{th},p}$, thereby raising the effective V_{th} .

Accordingly, we classify logic operations into two categories: set logic gates and reset logic gates. In a set logic gate, the device starts from logic “0”, and the write operation corresponds to the set process, whereby the device switches to logic “1” through threshold switching. In a reset logic gate, the output cell starts from logic “1”, and the write operation corresponds to the reset process, whereby the device is driven back to logic “0.” Thus, whether the set or reset transition serves as the write operation is determined jointly by the polarity relationship between $V_{\text{th},p}$ and $V_{\text{th},n}$ and the enforced initial state of the device.

To quantitatively validate the feasibility of logic operations, we next examined the resistance characteristics of the SOM device under both off-state and on-state conditions, as summarized in Supplementary Figure S10c–S10f. In the off-state, resistance values were obtained using DC sweeps because the current level before threshold switching was too low to be reliably captured by the OSC. As shown in Figure S10c and S10d, the measured resistance exceeded $10^6 \text{ }\Omega$ for both resistance configurations of 400 Ω and 10 k Ω , confirming that the SOM maintains sufficiently high isolation in the nonconductive regime. This ensures negligible leakage and provides a clear separation for defining logic “0.”

In the on-state, the transient resistance response during pulse application was recorded. For these measurements, voltage pulses with an amplitude of 5 V, rise and fall times of 10 ns, and a pulse width of 1 μs were applied. Figure S10e and S10f illustrate the abrupt resistance drop associated with threshold switching, followed by saturation during the remainder of the pulse. The initial sharp transition reflects the RC delay inherent to the circuit, after which the resistance stabilizes at a relatively low value. Notably, the stabilized-on resistance depended on the polarity condition: approximately 1 k Ω for the 400 Ω case (Figure S10e) and 5 k Ω for the 10 k Ω case (Figure S10f). These results indicate that the observed variation in the on-resistance level arises primarily from the different series resistance conditions imposed during operation.

Together, the ultrahigh off-resistance ($\geq 10^6 \text{ }\Omega$) and the polarity-dependent but stable on-resistance (1–5 k Ω) ensure a robust

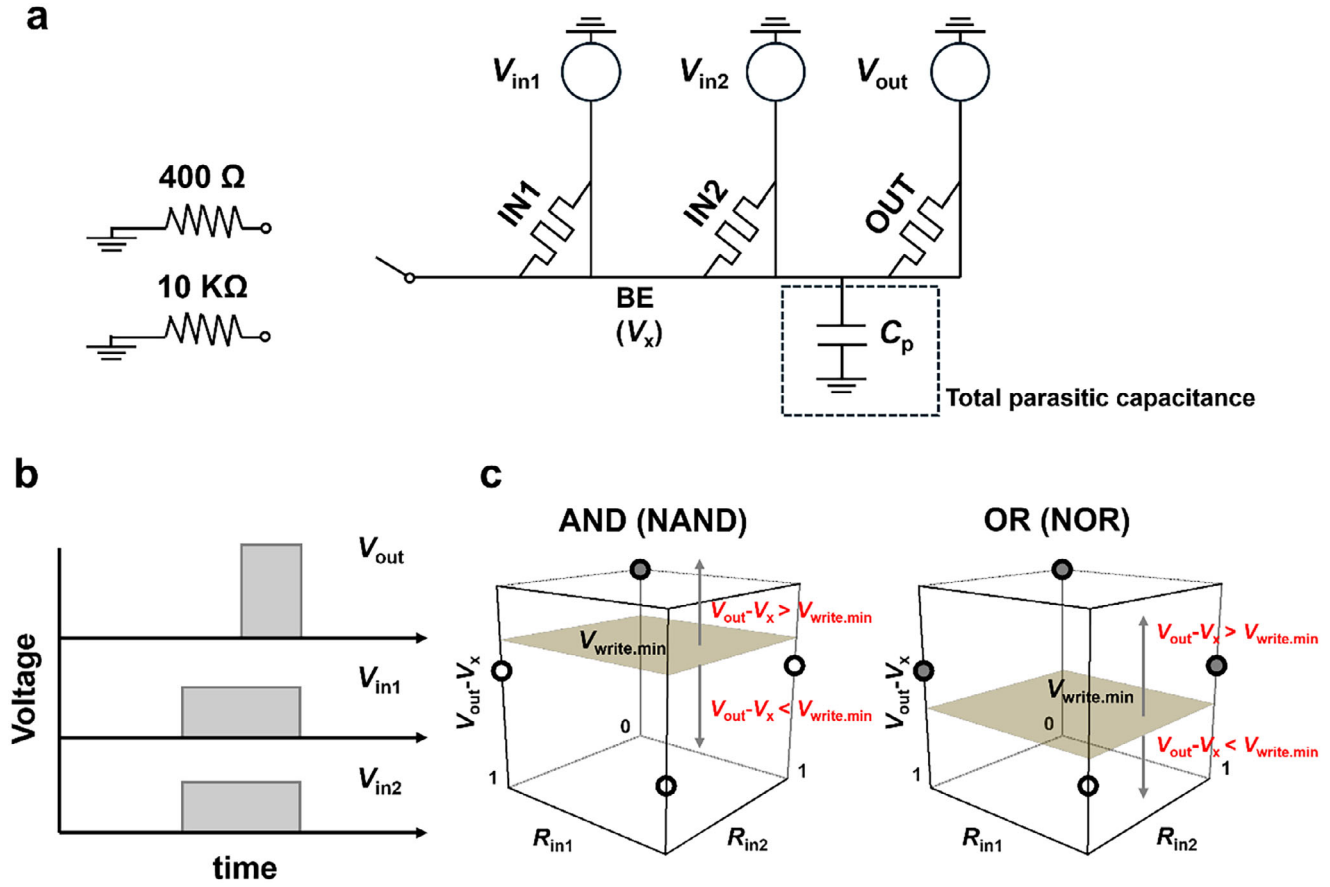


FIGURE 4 | (a) Circuit configuration for logic operation using SOM devices, consisting of two input nodes V_{in1} , V_{in2} and one output node V_{out} with series resistances (400 or 10 k Ω) and parasitic capacitance C_p . (b) Timing diagram of the applied input and output voltages during logic operation. (c) Logic scheme of SOM devices, where switching occurs if $(V_{out} - V_x) > V_{write.min}$ (filled circles) and is suppressed otherwise (open circles). Depending on input amplitudes and initial states, the same circuit can realize AND/NAND or OR/NOR functions.

readout margin between logic “0” and logic “1”, thereby validating the device’s suitability for reliable stateful logic execution.

Figure 4a shows the circuit configuration implemented for stateful logic operations [18]. The top electrodes (TEs) of multiple SOM devices were individually connected to voltage sources, while all bottom electrodes (BEs) were tied together to a common node. (as shown in Figure 1b) This node was connected to ground through a selectable series resistor, enabling control over the switching polarity. The logic operations were performed by using the SOM devices at IN1 and IN2 as inputs to modulate the state of the SOM device at OUT, where the output state reflects the logical combination of the two inputs according to the applied pulse sequence. In this configuration, the parasitic capacitance arising from the device structure, wiring, and probe pads contributes to transient voltage behavior during pulse application, affecting the post-pulse relaxation across the SOM. The series resistor was set to either 400 or 10 k Ω to examine the impact of resistance on polarity control and logic operation stability. This setup emulates a single row of a crossbar array, in which multiple devices share a common line, allowing investigation of array-level stateful logic functionality. The voltage V_x at the common BE node during logic operation can be determined from Kirchhoff’s current law

as Equation (1) [39, 40].

$$\frac{V_x}{R_{series}} + \frac{V_x - V_{in1}}{R_{in1}} + \frac{V_x - V_{in2}}{R_{in2}} + \frac{V_x - V_{out}}{R_{out}} = 0, \quad (1)$$

From Equation (1), V_x can be expressed as Equation (2).

$$V_x = \frac{V_{in1}R_{in2}R_{out} + V_{in2}R_{in1}R_{out} + V_{out}R_{in1}R_{in2}}{R_{series}R_{in1}R_{in2} + R_{series}R_{in2}R_{out} + R_{series}R_{in1}R_{out} + R_{in1}R_{in2}R_{out}} R_{series} \quad (2)$$

Here, R_{series} is the selectable external series resistance, R_{in1} and R_{in2} are the instantaneous resistances of the input SOM devices, R_{out} is the resistance of the output device, V_{in1} and V_{in2} are the input voltages, and V_{out} is the voltage applied to the OUT device. Since the effective voltage across the output SOM during logic operation is given by $(V_{out} - V_x)$, whether this applied voltage exceeds the write threshold directly determines if the SOM undergoes logic state switching, thereby defining the outcome of the logic operation.

Figure 4b illustrates the timing scheme used for pulse application during stateful logic operations. In SOM devices, the V_{th} state determines the voltage level required for switching, but at low bias voltages both the high- V_{th} and low- V_{th} states exhibit similarly

low current due to the steep turn-on behavior of the device. Therefore, to reliably exploit the large conductance contrast between on and off states during logic operations, the input cells (IN1 and IN2) were biased earlier than the output cell within the same operation cycle, using pulses with a longer duration. In this scheme, the pulses for IN1 and IN2 start before the pulse for OUT and remain active during its application, ensuring that the input devices have already reached their intended conductance states by the time the output cell is programmed. To achieve this, a deliberate time delay was introduced between the input and output pulses, taking into account the intrinsic switching speed of the SOM when transitioning from the off-state to the on-state, and the RC delay associated with the device's resistance-capacitance response, which governs the time required for the device to reach a stable low-resistance state. This sequencing prevents unintended voltage division and ensures that the output cell experiences the correct programming conditions derived from the conductive states of the input cells.

Figure 4c schematically illustrates the logic determination principle based on the relative magnitude of the applied programming voltage across the SOM device. Specifically, writing occurs only when the effective voltage drop across the output device, defined as $(V_{\text{out}} - V_x)$, exceeds the minimum writing threshold voltage ($V_{\text{write.min}}$). Here, $V_{\text{write.min}}$ represents the minimum voltage required for a write operation to occur, below which no state change is induced. Since V_{out} is fixed in this study, the logic behavior is determined by how V_x is established through Equation (2), and the resulting value of $(V_{\text{out}} - V_x)$ dictates whether a write event takes place.

For intuitive analysis, the resistance of the SOM devices in their high-resistance off-state is approximated as infinite, simplifying the evaluation of V_x . Here, the device states are denoted as (IN1, IN2, OUT), where each entry corresponds to the logic level of the respective SOM cell. Under this assumption, the resulting expressions for V_x were derived for the four representative logic states, namely (0,0,0), (0,1,0), (1,0,0), and (1,1,0). These cases are summarized in Equation (3–6).

$$(R_{\text{in1}}, R_{\text{in2}}, R_{\text{out}}) = (0, 0, 0) \rightarrow V_x = 0 \quad (3)$$

$$(R_{\text{in1}}, R_{\text{in2}}, R_{\text{out}}) = (0, 1, 0) \rightarrow V_x = \frac{R_{\text{series}} V_{\text{in2}}}{R_{\text{series}} + R_{\text{in2}}} \quad (4)$$

$$(R_{\text{in1}}, R_{\text{in2}}, R_{\text{out}}) = (1, 0, 0) \rightarrow V_x = \frac{R_{\text{series}} V_{\text{in1}}}{R_{\text{series}} + R_{\text{in1}}} \quad (5)$$

$$(R_{\text{in1}}, R_{\text{in2}}, R_{\text{out}}) = (1, 1, 0) \rightarrow V_x = \frac{R_{\text{in2}} V_{\text{in1}} + R_{\text{in1}} V_{\text{in2}}}{R_{\text{series}} R_{\text{in1}} + R_{\text{series}} R_{\text{in2}} + R_{\text{in1}} R_{\text{in2}}} R_{\text{series}} \quad (6)$$

By comparing $(V_{\text{out}} - V_x)$ with $V_{\text{write.min}}$, one can directly predict whether writing will occur under each input condition. In the schematic representation, filled circles denote input conditions where $(V_{\text{out}} - V_x) > V_{\text{write.min}}$ and writing is successfully

induced, while open circles indicate conditions where $(V_{\text{out}} - V_x) < V_{\text{write.min}}$, and the device state remains unchanged. For the case of $R_{\text{series}} = 400 \Omega$, the initial state is defined as logic “0”, and writing corresponds to a transition into logic “1.” When the device state is (0,0,0), V_x becomes zero, and thus the entire V_{out} is applied across the output device, exceeding $V_{\text{write.min}}$ and inducing a switching event that changes the state to logic “1.” In contrast, when the device state is (1,1,0), V_x attains the largest value among the four cases. By appropriately selecting V_{in1} and V_{in2} , V_x can be made sufficiently large so that the effective voltage drop $(V_{\text{out}} - V_x)$ does not surpass $V_{\text{write.min}}$, thereby suppressing switching and maintaining the logic “0” state. For the device states (1,0,0) and (0,1,0), the resulting V_x takes an intermediate value between the (0,0,0) and (1,1,0) cases. In the (1,0,0) condition, V_x is primarily determined by V_{in1} , since the second input remains in the high-resistance state and contributes negligibly. Conversely, in the (0,1,0) condition, V_x is governed by V_{in2} under the same reasoning. Whether switching occurs in these cases therefore depends on the specific magnitude of the active input voltage: if the applied V_{in} is sufficiently low, V_x remains small, allowing $(V_{\text{out}} - V_x)$ to exceed $V_{\text{write.min}}$ and trigger switching, thereby realizing a NAND operation. If V_{in} is set higher, V_x increases, $(V_{\text{out}} - V_x)$ falls below $V_{\text{write.min}}$, and switching is suppressed, leading instead to a NOR operation. Thus, by appropriately tuning the input voltages in this configuration, both NAND and NOR logic functions can be achieved within the same circuit framework.

On the other hand, when the series resistance is $R_{\text{series}} = 10 \text{ k}\Omega$, the device is initialized in logic “1”, and the write process corresponds to resetting the cell to logic “0.” In this case, the voltage across the output device, given by $(V_{\text{out}} - V_x)$, follows the same dependence on the device states as described earlier, but the resulting logic mapping is reversed. Specifically, when the device state is (0,0,1), V_x is minimized, so $(V_{\text{out}} - V_x)$ readily exceeds $V_{\text{write.min}}$ and the output resets to logic “0.” When the device state is (1,1,1), V_x reaches its maximum value, suppressing switching and preserving the output at logic “1.” For the states (1,0,1) and (0,1,1), V_x takes intermediate values determined by the active input, and the outcome depends on the applied V_{in} amplitude. If V_{in} is low enough to keep V_x small, $(V_{\text{out}} - V_x)$ surpasses $V_{\text{write.min}}$ and the output resets, producing an AND operation. Conversely, if V_{in} is higher, V_x increases and switching is suppressed, so only the (0,0,1) case induces a reset, yielding an OR operation. Thus, while the 400Ω configuration enables NAND and NOR operation through set-based transitions, the $10 \text{ k}\Omega$ configuration realizes AND and OR operation through reset-based transitions, suggesting the dual functionality achievable within the same SOM architecture.

Based on the circuit configuration and pulse scheme described above, we implemented stateful logic operations using the SOM devices. As shown in Figure 5a, the IMPLY operation requires one input device and one output device. Therefore, two SOM cells were employed, with a series resistance of 400Ω connected to the common bottom electrode node. The governing Kirchhoff's current law for this circuit is identical to Equation (7), and the corresponding voltage drop across the output device, $(V_{\text{out}} - V_x)$, was calculated according to Equation (8).

$$\left(\frac{1}{R_{\text{series}}} + \frac{1}{R_{\text{in1}}} + \frac{1}{R_{\text{out}}} \right) V_x = \frac{V_{\text{in1}}}{R_{\text{in1}}} + \frac{V_{\text{out}}}{R_{\text{out}}} \quad (7)$$

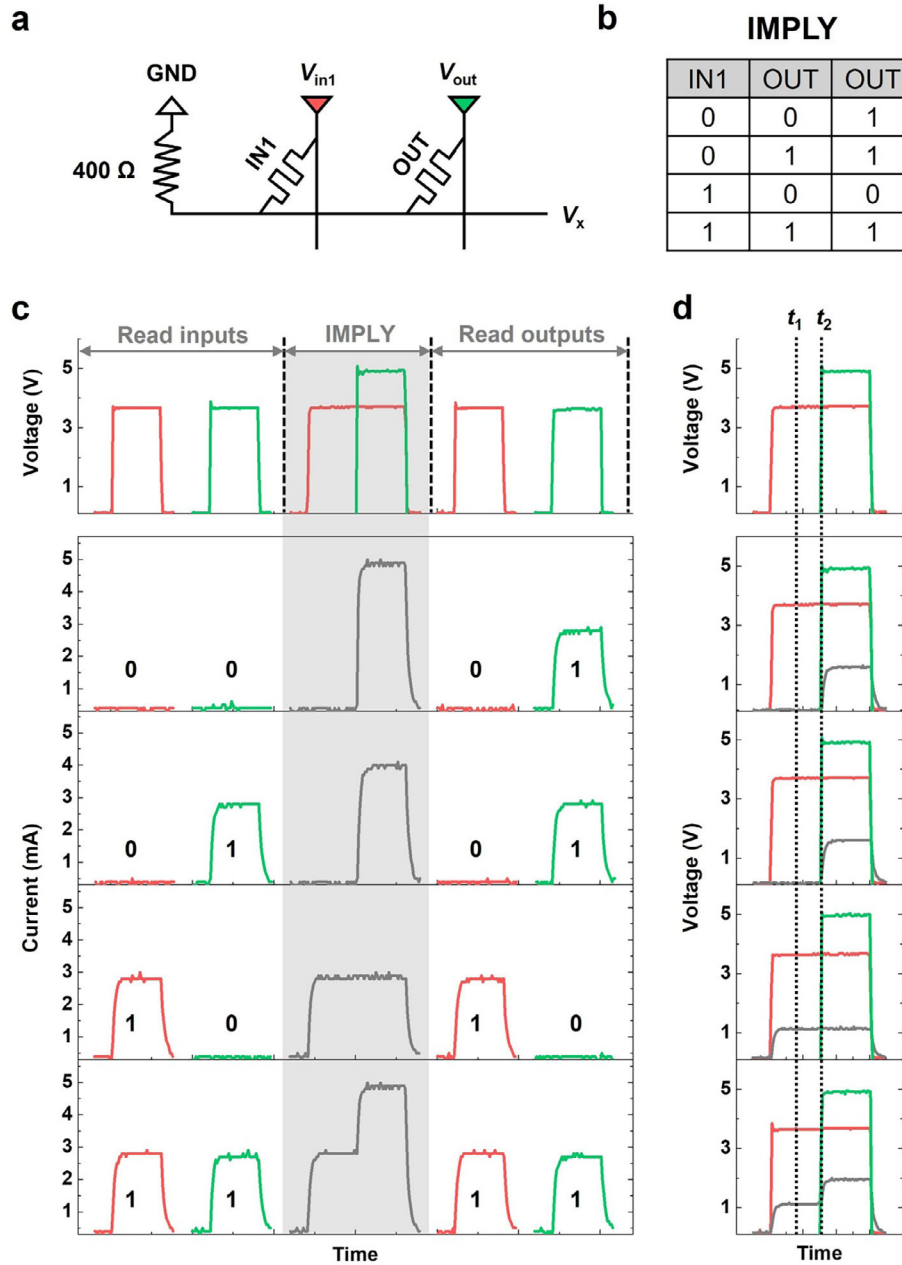


FIGURE 5 | (a) Circuit configuration for IMPLY logic operation using SOM devices, where the input V_{in1} and output V_{out} nodes are controlled with a series resistance of $400\ \Omega$. (b) Truth table of the IMPLY logic function. (c) Experimental demonstration of the IMPLY logic gate in the SOM circuit. input (red) and output (green) voltages, node voltage (gray), and corresponding device currents, confirming correct logic states for all input combinations. (d) Time-resolved measurement of the node voltage V_x together with V_{in1} and V_{out} , showing its transient evolution during the IMPLY sequence (t_1 : input activation, t_2 : output programming).

$$V_{out} - V_x = V_{out} - \frac{R_{series} (V_{in1} R_{out} + V_{out} R_{in1})}{R_{in1} R_{out} + R_{series} R_{in1} + R_{series} R_{out}} \quad (8)$$

The truth table for IMPLY logic is provided in Figure 5b. For the experimental conditions, the output voltage was set to 5 V, the high-resistance off-state was approximated as infinite resistance, and the low-resistance on-state was fixed at 1 k Ω . Under these assumptions, the operational read voltage was set to 3.7 V, and the input voltages were also fixed at the same level, ensuring consistent biasing conditions and reliable distinction of logic states.

As shown in Figure 5c, the logic results of the SOM devices were consistent with the IMPLY truth table under all input combinations. In this panel, the red color denotes V_{in1} with its corresponding voltage and current, the green color denotes V_{out} with its voltage and current, and the gray color indicates the node voltage V_x , along with the corresponding current reflecting logic transitions. Prior to executing the logic operation, an initial read pulse was applied to verify the device state by confirming the presence or absence of threshold switching. After the logic operation, another read pulse was applied to confirm the updated logic state of the device.

In our implementation, each read pulse was applied with a duration of 3 μ s. For logic operations, the input pulse was applied with a duration of 6 μ s and the output pulse with a duration of 3 μ s, such that the onset of the output pulse was delayed by 3 μ s relative to the input pulse. This delay provides a sufficiently long time interval compared with the intrinsic device dynamics: as shown in Figure S4 the intrinsic switching speed of SOM devices is below 50 ns, while Figure S10 demonstrates that the gradual relaxation induced by RC delay saturates within approximately 1 μ s. Therefore, the chosen 3 μ s delay ensures that both the threshold switching event and resistance stabilization are fully completed before the subsequent programming step, guaranteeing reliable execution of the IMPLY operation.

Figure 5d shows the time-dependent evolution of the node voltage V_x . At t_1 , a bias pulse is applied to the IN1 device to initiate its activation, whereas the OUT cell remains unbiased at this stage. When the initial state of IN1 is “0”, its higher threshold voltage prevents switching, and no transition is observed. In contrast, if the initial state is “1”, the lower threshold voltage allows threshold switching to occur, which is clearly observed in the transient response.

At t_2 , once the output programming pulse is applied, the effective programming voltage across the output device ($V_{out}-V_x$) determines whether the SOM undergoes switching. If the applied voltage is insufficient, no threshold switching is triggered and the output retains its prior state. If it exceeds the switching condition, threshold switching occurs and the output is updated. However, it should be noted that the actual switching behavior also depends on the initial threshold level of the output device. For example, under the device state (IN1, OUT) = (1,0), if the output device is initially in logic “0”, the applied voltage may not be sufficient to induce threshold switching, whereas in the (IN1, OUT) = (1,1) condition, the lower initial V_{th} of the output device can enable switching under the same bias. Through this mechanism, the IMPLY operation is successfully executed in accordance with the designed logic scheme.

Building upon the circuit configuration shown in Figure 6a, consisting of two input devices (IN1 and IN2) and one output device connected through a 400 Ω series resistor, we implemented multi-input logic gate operations. The corresponding truth tables for NAND and NOR operations are presented in Figures 6b and 6c, respectively. To determine the appropriate pulse amplitudes for the input devices, we first performed a theoretical analysis of the switching conditions. Using the expression for V_x described in Equations (3–6), and by substituting experimentally relevant parameters ($V_{out} = 5$ V, $R_{off} \approx \infty$, and $R_{on} \approx 1.1$ k Ω , $R_{series} \approx 400$ Ω), the effective node voltage V_x was calculated for different input states. For simplicity, we proceed under the assumption that $V_{in1} = V_{in2} = V_{in}$.

When the devices were in the high-resistance state (0,0,0), the node potential was $V_x = 0$, giving the maximum programming bias across the output device ($V_{out}-V_x$) = 5 V. Since the output device is biased with a voltage almost equal to the applied write pulse, this value consistently exceeds $V_{write,min}$, ensuring a state transition into logic “1.” In the device states (1,0,0) and (0,1,0), the node voltage was found to be $V_x = \frac{4}{15}V_{in1}$ or $V_x = \frac{4}{15}V_{in2}$,

respectively. Depending on the applied V_{in} amplitude, ($V_{out}-V_x$) may exceed or fall below $V_{write,min}$. For the (1,1,0) state, both input resistances contribute, resulting in a larger node potential of $V_x = \frac{4}{19}(V_{in1} + V_{in2})$, which reduces the effective output voltage.

The logic outcome depends critically on whether ($V_{out}-V_x$) exceeds $V_{write,min}$. If writing occurs for (0,0,0), (1,0,0), and (0,1,0) but is suppressed in the (1,1,0) condition, the output switches to “1” in the first three cases and remains “0” in the last, corresponding to NAND logic. This requires satisfying the inequalities $(5-\frac{4}{15}V_{in}) > V_{write,min}$ and $(5-\frac{8}{19}V_{in}) < V_{write,min}$, which together define the allowable range of input amplitude as $\frac{19}{8}(5-V_{write,min}) < V_{in} < \frac{15}{4}(5-V_{write,min})$. Conversely, if writing occurs solely to the (0,0,0) case, with the states (0,1,0), (1,0,0), and (1,1,0) suppressed, the truth table corresponds to NOR logic. This condition is realized when $(5-\frac{4}{15}V_{in}) < V_{write,min}$ and $(5-\frac{8}{19}V_{in}) < V_{write,min}$, which simplifies to $V_{in} > \frac{15}{4}(5-V_{write,min})$.

Thus, by carefully choosing the amplitude of the input voltages, the same physical configuration can reproducibly execute either NAND or NOR operations. In this analysis, the $V_{write,min}$ was set equal to $V_{th,n}$ because programming does not occur for amplitudes below $V_{th,n}$, whereas application of a bias exceeding $V_{th,n}$ triggers threshold switching and consequently induces the transition from the $V_{th,n}$ state to the $V_{th,p}$ state. Based on this definition and assuming $V_{write,min} = 4$ V, the derived inequalities indicate that NAND functionality can be realized when 2.375 V $< V_{in} < 3.75$ V, whereas NOR functionality is obtained when $V_{in} > 3.75$ V. As experimentally demonstrated in Figures 6d and 6e, NAND and NOR operations were reliably obtained by selecting $V_{in} = 3.5$ V and $V_{in} = 3.9$ V, respectively, in excellent agreement with the theoretical predictions.

Building upon the 10 k Ω series resistance configuration, we next investigated the realization of AND and OR logic operations, with the circuit diagram shown in Figure 7a and the corresponding truth tables summarized in Figures 7b and 7c. In this case, the polarity condition corresponds to $V_{th,p} > V_{th,n}$, and thus the device was initialized to logic “1”, with writing defined as the reset operation to logic “0.” For the experiments, the read pulse was applied with an amplitude of 2.8 V and a duration of 1 μ s. During the logic operation, the output pulse was applied with a duration of 1 μ s, while the input pulses were applied with a duration of 4 μ s. The onset of the output pulse was delayed by 3 μ s relative to the input pulses, ensuring the correct sequencing of logic execution. To theoretically determine the switching conditions, the effective node voltage V_x was derived from Equations (3–6) for each input state, while setting the circuit parameters to experimentally relevant values ($V_{out} = 5$ V, $R_{off} \approx \infty$, and $R_{on} \approx 5$ k Ω , $R_{series} \approx 10$ k Ω). When the device state is (0,0,1), the node voltage collapses to zero, so the applied programming bias across the output device reaches the full V_{out} amplitude, inevitably exceeding the writing threshold and resetting the device to logic “0.”

For the mixed states (1,0,1) and (0,1,1), the node voltage V_x becomes $\frac{2}{3}V_{in1}$ or $\frac{2}{3}V_{in2}$, such that the effective programming bias is reduced to $(5-\frac{2}{3}V_{in})$. When switching occurs in these cases

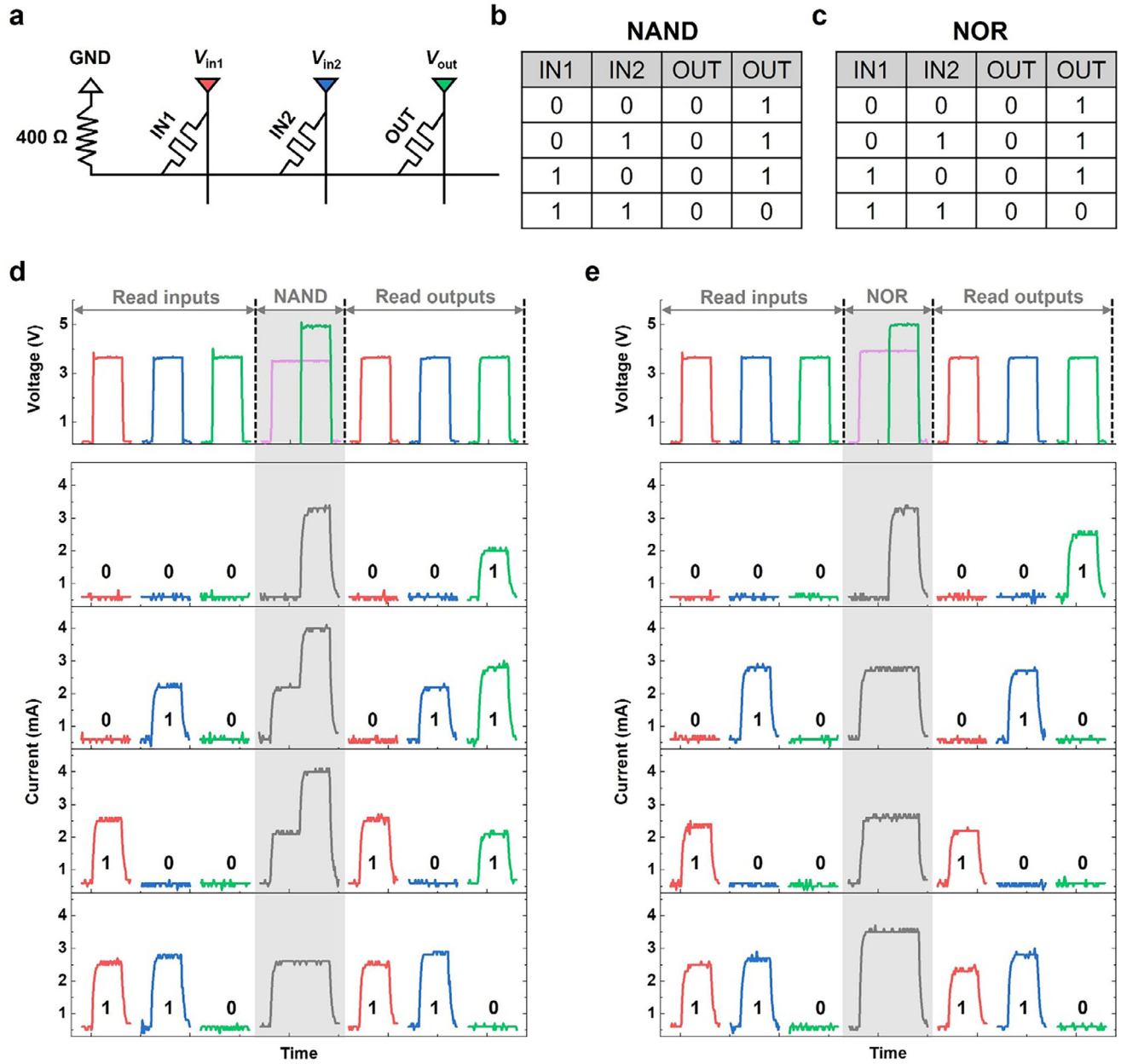


FIGURE 6 | (a) Circuit configuration for two-input logic operation using SOM devices with a 400 Ω series resistance. (b,c) Truth tables of NAND and NOR logic functions, respectively. (d) Experimental NAND operation. The output switches only for device states (IN1, IN2, OUT) = (0,0,0), (0,1,0), and (1,0,0), while remaining unchanged for (1,1,0), reproducing the NAND truth table. (e) Experimental NOR operation. The output switches exclusively for the device state (IN1, IN2, OUT) = (0,0,0), while other states remain unchanged, corresponding to the NOR truth table.

but is inhibited in the (1,1,1) state, the output behavior matches that of an AND gate. Conversely, if switching is suppressed for both the mixed states and the (1,1,1) state, only the (0,0,1) condition induces a reset, thereby reproducing an OR operation. For the (1,1,1) state, both input channels conduct simultaneously, raising the node potential to $V_x = \frac{2}{5}(V_{in1} + V_{in2})$. This is the largest value among all input combinations, and thus the effective programming bias ($V_{out} - V_x$) becomes the smallest.

To realize an AND operation, the mixed-input states (1,0,1) and (0,1,1) must undergo switching while the (1,1,1) state remains unswitched. This condition requires that $(5 - \frac{2}{3}V_{in}) > V_{write,min}$

and $(5 - \frac{4}{5}V_{in}) < V_{write,min}$ are simultaneously satisfied, which simplifies to the inequality $\frac{5}{4}(5 - V_{write,min}) < V_{in} < \frac{3}{2}(5 - V_{write,min})$. Conversely, to realize an OR operation, (0,0,1) state must undergo switching while all other states—(1,0,1), (0,1,1), and (1,1,1)—remain unswitched. This requires that both $(5 - \frac{2}{3}V_{in}) < V_{write,min}$ and $(5 - \frac{4}{5}V_{in}) < V_{write,min}$ hold true, which reduces to the condition $V_{in} > \frac{3}{2}(5 - V_{write,min})$.

Experimentally, $V_{write,min}$ was defined as the minimum voltage required to reliably induce the intended write operation. Under the 10 k Ω condition, threshold switching can occur

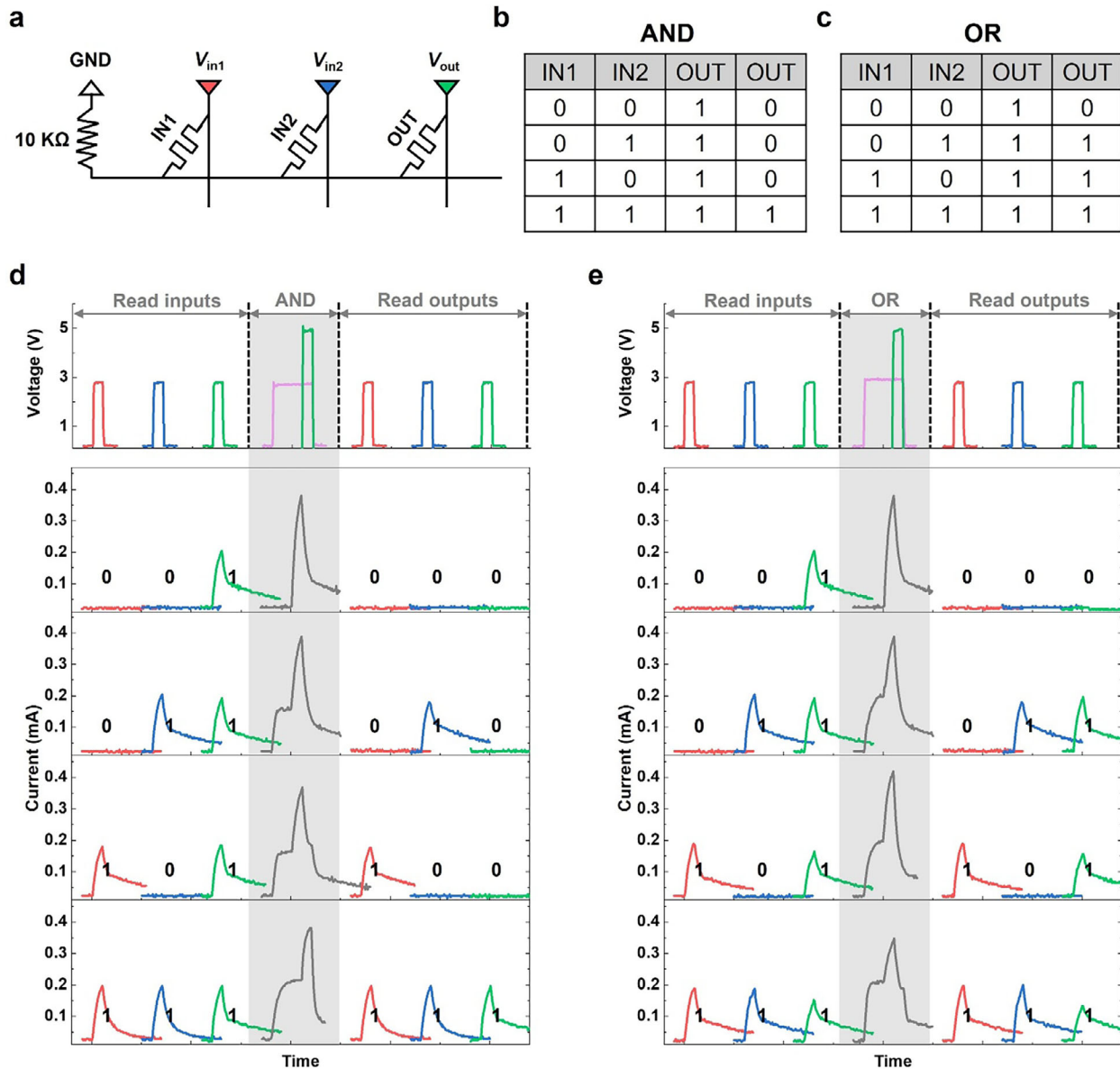


FIGURE 7 | (a) Circuit configuration for two-input logic operation using SOM devices with a 10 k Ω series resistance. (b,c) Truth tables of AND and OR logic functions, respectively. (d) Experimental AND operation. The output resets only for device states (IN1, IN2, OUT) = (0,0,1), (0,1,1), and (1,0,1), while remaining unchanged for (1,1,1), consistent with the AND truth table. (e) Experimental OR operation. The output resets exclusively for the (0,0,1) device state, while other states remain unchanged, reproducing the OR truth table.

even within the read-voltage range, and repeated switching events may progressively modify the threshold-voltage state. Therefore, the onset of threshold-state degradation was adopted as the practical criterion for determining $V_{\text{write,min}}$. Accordingly, $V_{\text{write,min}}$ was set to 3.1 V, and the analysis confirmed that AND operation could be realized when the input amplitude satisfied $2.375 \text{ V} < V_{\text{in}} < 2.85 \text{ V}$, while OR operation was obtained for $V_{\text{in}} > 2.85 \text{ V}$.

As shown in Figures 7d and 7e, the experimental waveforms verified these conditions: when V_{in} was set to 2.7 V within the predicted range, the device states (1,0,1) and (0,1,1) switched while the (1,1,1) state remained unswitched, reproducing the AND truth table in Figure 7d. Conversely, at $V_{\text{in}} = 2.9 \text{ V}$ above the threshold, only the (0,0,1) state underwent switching while all

other states were suppressed, consistent with OR logic behavior in Figure 7e. These results confirm stable and reproducible AND and OR gate operations, in excellent agreement with the theoretical predictions.

Taken together, the results from Figures 5–7 demonstrate the programmability of logic functionality in SOM-based circuits by controlling the series resistance and initial output state. Specifically, when the circuit is configured with a 400 Ω resistor, set-type logic gates such as IMPLY, NAND, and NOR are realized, while with a 10 k Ω resistor, reset-type logic gates such as AND and OR are obtained. This dual-mode capability underscores the flexibility of SOM devices for implementing a complete set of universal logic operations within a compact and reconfigurable hardware framework.

2.3 | Demonstration of Half-Adder Logic Circuit

To further validate the feasibility of cascading logic operations in the proposed SOM devices, we implemented a half-adder circuit using the previously demonstrated logic gates. A half-adder is a fundamental combinational logic block that generates a SUM and a CARRY output from two binary inputs [19, 41]. Conventionally, it can be realized using a combination of one AND gate and one XOR gate (or equivalently, NAND/NOR-based structures) [42, 43].

In this work, the half-adder was constructed under the 400 Ω series resistance condition ($V_{th,p} < V_{th,n}$). Instead of employing conventional AND/XOR gates, we designed the circuit using only IMPLY and NAND operations, thereby demonstrating the versatility and universality of the SOM-based stateful logic framework. The logic network required a total of seven SOM cells and proceeded through five sequential operation steps.

The schematic representation of the circuit is shown in Figure 8a [19]. Two devices, labeled IN1 and IN2, served as the primary inputs to the half-adder. Three additional intermediate devices (IN3, IN4, IN5) were introduced to store and process intermediate logic states. Finally, two dedicated devices acted as the output elements, providing the SUM and CARRY values. A fixed 400 Ω resistor was connected in series with the network to maintain the desired switching dynamics.

The sequence of logical operations executed across the five steps is summarized in Figure 8b. The design employed a total of four NAND and one IMPLY operations to generate the complete half-adder functionality. Each step produced intermediate results in the auxiliary devices, which were subsequently used as inputs to the following step. The cascading of these operations confirmed that multistage computation can be stably realized in this SOM-based architecture.

The corresponding electrical measurements are presented in Figure 8c. The top panel shows the voltage waveforms applied to each device during the sequential operations, while the lower four panels plot the measured current responses. In each logic step, the current flowing through the input, intermediate, and output devices was monitored to determine their logic states. The “Read input” and “Read output” regions represent the current levels measured under read pulses to verify the logic state of each device. The shaded regions denote the logic execution windows, where the voltage difference across the output device ($V_{out} - V_x$) exceeded $V_{write,min}$, thereby inducing state transitions. In these plots, IN1, IN2, SUM, and CARRY are color-coded as red, blue, yellow, and green, respectively, while the intermediate devices are shown in gray. Importantly, the experimental results confirmed that the output devices correctly transitioned according to the expected truth table, yielding stable SUM and CARRY outputs. Overall, the demonstration validates that SOM-based stateful logic devices are capable of cascaded multistep operations, not limited to elementary gates but extending to compound logic circuits. The stable realization of the half-adder further highlights the potential of this platform for constructing more complex arithmetic units, and ultimately full adders, using compact two-terminal SOM devices and simple resistive networks.

Furthermore, the demonstrated half-adder provides experimental evidence that the load-resistance conditions identified from single-device measurements remain effective in cascaded logic architectures. Despite the involvement of seven interconnected SOM devices and five sequential logic-operation steps, reliable logic functionality was maintained throughout the computation process, indicating sufficient robustness for multistage logic execution within the proposed SOM-based architecture.

Table 1 provides a comparative summary of experimental demonstrations of logic-in-memory using various emerging memory technologies, including RRAM, PCRAM, and the SOM developed in this work. Previous studies on RRAM-based stateful logic have demonstrated functions such as IMPLY, NIMP, AND, OR, and NOR with pulse durations ranging from a few microseconds to hundreds of microseconds, depending on the oxide material system employed [20, 44, 45]. Similarly, PCRAM-based demonstrations have shown reliable NOT, IMPLY, OR, and NIMP operations with shorter pulse durations on the order of tens of nanoseconds [18, 46]. Recent logic-in-memory platforms based on FeFETs, FBFETs, and gated silicon diodes have also demonstrated various operations and improved energy efficiency. While these approaches provide important validation of logic-in-memory in different device classes, each platform involves trade-offs in operating speed, device structure, scalability, or integration complexity.

In contrast, the SOM device presented in this work offers several key advantages. The pulse width required for stable SOM-based operations is on the order of 6 μ s, which, while longer than the fastest PCRAM demonstrations, is still significantly shorter than the hundreds of microseconds reported for certain RRAM-based approaches. Moreover, the intrinsic switching dynamics (as shown in Figure S4) reveal sub-50 ns response times, indicating that the experimentally applied pulse widths are far from the device's physical speed limit. This suggests that, with further circuit optimization, SOMs can compete with PCRAM in terms of high-speed operation while maintaining superior logic versatility. The SOM exhibits an off-resistance greater than $10^6 \Omega$, which is comparable to or higher than most prior demonstrations. This ensures a clear distinction between logic states during both read and write operations, thereby minimizing leakage and misread errors, for instance, an issue that often plagues oxide-based RRAM devices with relatively low off-state resistance. The SOM does not require an additional access transistor or selector, unlike conventional RRAM or PCRAM crossbar implementations. This selector-free operation enables reliable logic functionality even in large-scale arrays, ensuring high integration density beyond simple single-line configurations [25]. Such structural simplicity not only reduces fabrication complexity but also facilitates straightforward array-level scaling for future logic-in-memory architectures.

3 | Conclusion

A SOM device based on SGST was experimentally demonstrated, exhibiting a unique capability of tunable operation directionality. The direction of threshold switching could be reversibly adjusted by varying the external series resistance, which modifies the transient RC dynamics during pulse application and results in

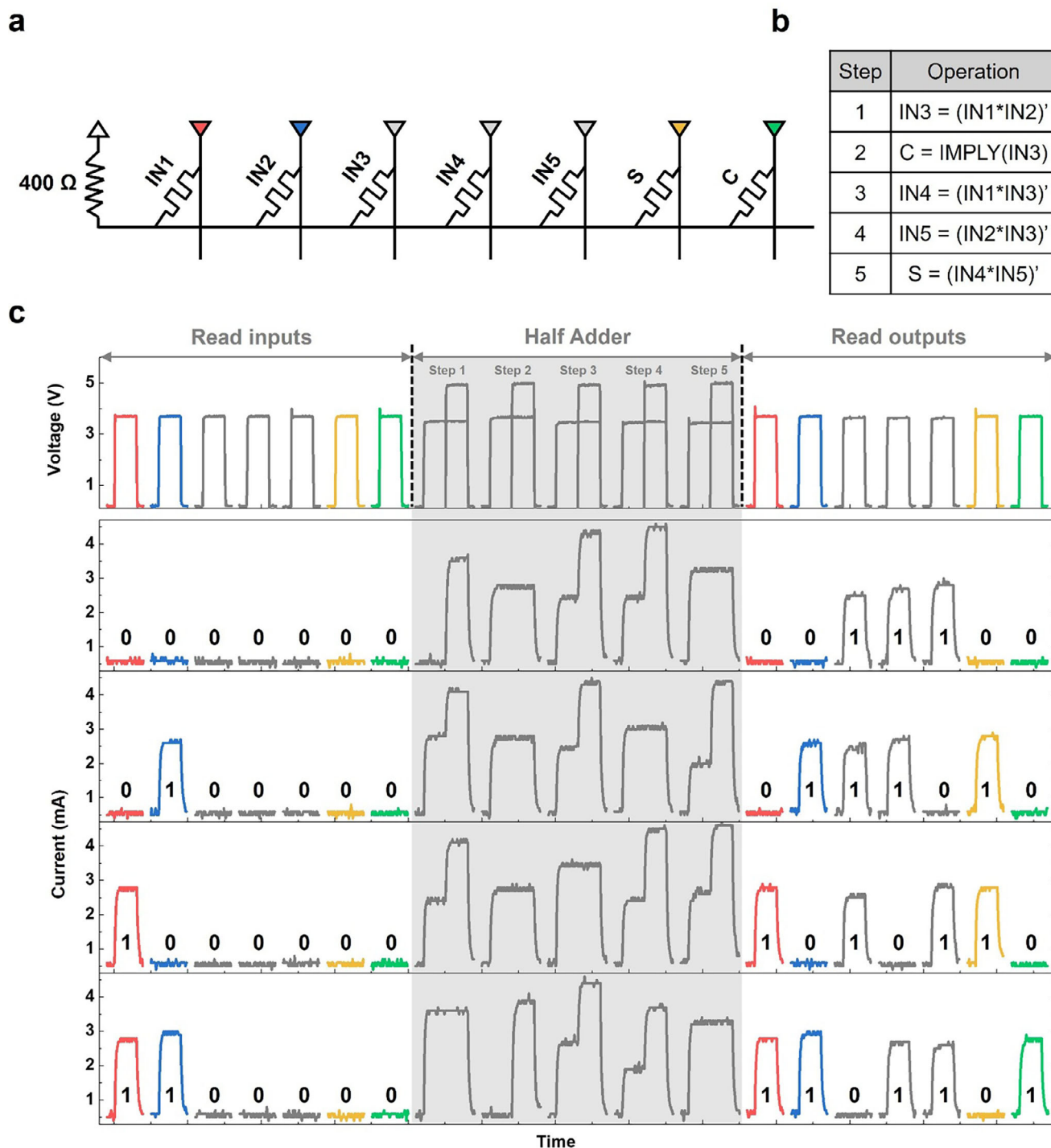


FIGURE 8 | (a) Circuit schematic of the SOM-based half-adder consisting of seven devices: two primary inputs (IN1, IN2), three intermediate nodes (IN3–IN5), and two outputs for sum (S) and carry (C). A 400 Ω series resistor was included to control the switching dynamics. (b) Operation sequence of the half-adder, summarized in five steps. Intermediate nodes IN3–IN5 are generated, followed by the evaluation of the carry (C) and sum (S) bits using combinations of NAND and IMPLY operations. (c) Experimental demonstration of the half-adder. Top panel shows the applied voltage waveforms, and lower panels present the measured current responses of all devices. The extracted logic states confirm correct operation of both S and C outputs for all four input combinations, validating cascaded multistep computation within the SOM array.

polarity-dependent modulation of the effective switching threshold. The device further showed high resistance contrast and strong nonlinearity, enabling stable switching. These intrinsic properties, combined with the simple two-terminal capacitor-like structure, eliminate the need for auxiliary selector elements and offer strong prospects for high-density integration.

Building upon these device characteristics, we implemented a complete set of stateful logic operations, including IMPLY, NAND, NOR, AND, and OR gates, within the same SOM-based architecture. By tailoring the input pulse amplitudes and external resistance, distinct logic functionalities could be selectively enabled, highlighting the reconfigurable and versatile nature of

TABLE 1 | Experimental demonstrations of logic in memory with various memories.

Device type	Device configuration	Functions	Pulse duration for logic operation (μs)	Off resistance (Ω)	No. Steps	Energy consumption (nJ)	Layout area
RRAM	Pt/TiO ₂ /Pt [20]	IMPLY	2	$>10^6$	1	$<10^{-1}$	12F ²
RRAM	Ta/TaO _x /Pt [44]	IMPLY, NIMP, AND, OR, NOR	100	10^5	1	—	12F ²
RRAM	Pt/Ta ₂ O ₅ /W/Pt [45]	OR, NIMP	100	5×10^4 – 5×10^5	1	—	12F ²
PCRAM	TiN/GeSbTe/TiN [46]	NOT, AND	60 ~ 120	$>10^6$	2, 3	—	12F ²
PCRAM	W/GeSbTe/TiN [18]	NOT, IMPLY, NOR	1	10^5 – 10^6	1	—	12F ²
Diode	p ⁺ -n-p-n ⁺ GSD [19]	NAND, NOR	2 ~ 10	$>10^9$	1	$<5 \times 10^{-5}$	12F ²
FeFET	HfO _x -based FeFET [47]	NAND, NOR	<0.01	$>10^7$	2	$<10^{-8}$	—
FBFET	Triple-Gated NS-FBFET [48]	NAND, NOR	N/A	$\sim 10^7$	1	$<9 \times 10^{-2}$	—
SOM (This work)	W/GeSnSeTe/W	IMPLY, OR, AND, NOR, NAND	6	$>10^6$	1	<200	12F ²

SOM-based logic. The feasibility of cascading operations was confirmed through the successful implementation of a half-adder, demonstrating that multistage logic can be stably executed in this platform.

Compared with previous demonstrations of stateful logic in RRAM- and PCRAM-based devices, the proposed SOM approach offers clear advantages, including higher off-state resistance, stronger nonlinearity, and structural simplicity without the need for integrated selectors. These benefits directly address the long-standing challenges of sneak current, scalability, and circuit overhead in large-scale in-memory computing systems. Overall, the presented SOM framework establishes a promising pathway toward reconfigurable, energy-efficient, and highly scalable logic-in-memory architectures, making it a strong candidate for next-generation edge computing and beyond von Neumann systems.

4 | Experimental Section

4.1 | Device Fabrication

A SOM device was fabricated based on a SGST chalcogenide material, forming a two-terminal capacitor-like structure. The fabrication process began with the deposition of a 30-nm-thick tungsten bottom electrode onto a Si/SiO₂ substrate using direct current (DC) magnetron sputtering. The BE was patterned via photolithography and inductively coupled plasma reactive-ion etching (ICP-RIE), using Ar (4 sccm) and Cl₂ (30 sccm) as etching gases under a pressure of 5 mTorr, with an ICP source power of 300 W and substrate bias of 50 W. The etch rate was approximately 1 nm/min. Residual photoresist was removed

sequentially using acetone, isopropyl alcohol, and deionized water. The SGST active layer was deposited via radio frequency (RF) sputtering using separate Sn, GeSeTe, and GeTe targets at 20, 40, and 30 W, respectively. The process was carried out under a base pressure of 5×10^{-7} Torr and a working pressure of 3.3 mTorr with an Ar flow rate of 20 sccm. A 65-nm-thick W top electrode was then deposited by DC sputtering and patterned through photolithography, followed by a lift-off process. The TE deposition was performed under a base pressure of 1×10^{-6} Torr and a working pressure of 2.1 mTorr, with a DC power of 140 W and an Ar flow rate of 15 sccm.

4.2 | Material Analysis

Cross-sectional views of the SOM device were obtained using high-resolution transmission electron microscopy (HR-TEM; JEM-F200, JEOL). The fabricated SOM arrays were observed using field-emission scanning electron microscopy (FE-SEM; JSM-7800F, JEOL).

4.3 | Electrical Characterization

The current–voltage (I–V) sweep mode of an HP4155B semiconductor parameter analyzer was employed to measure the switchable threshold voltage characteristics of the device. DC measurements were used to characterize both the off-state current and the high-resistance state in the off-region, allowing precise evaluation of the switching behavior under static bias conditions. For pulse-based electrical characterization, the setup consisted of an AFG (Agilent 81150A), an OSC (MSOX3024T, Tektronix), an RF electrical circuit switch box, and an external

variable resistor. During all measurements, the voltage bias was applied to the W top electrode, with the W bottom electrode connected in series with an external variable resistor before ground, providing a controllable reference path. All write pulses were configured with an amplitude of 5 V and rise/fall times of 10 ns, enabling fast and reproducible switching. The programmed V_{th} was verified by applying a single triangular read pulse capable of capturing the exact threshold voltage of the device in its current state. This method enables accurate V_{th} measurement across all programmed states. For standard read operations, a triangular pulse with an amplitude of 6 V and rise/fall times of 40 μ s was employed to ensure complete signal capture.

Endurance characteristics were assessed by repeatedly applying two alternating write voltages. Throughout the cycling process, the V_{th} for both programmed states was intermittently measured using the triangular read pulse method. Retention measurements were conducted at an elevated temperature of 85°C to accelerate potential degradation mechanisms. Each V_{th} state was programmed using the write pulse and then monitored to confirm whether it was maintained for at least 2 h. The read pulse used in retention testing had an amplitude of 2.8 V, the same width as the write pulse, and rise/fall times of 10 ns to ensure consistent sensing conditions.

Additionally, the threshold voltage drift phenomenon—known to occur in ovonic threshold switching devices—was investigated in detail. After applying a write pulse, triangular read pulses were applied at elapsed times of 10^{-6} , 10^{-4} , 10^{-2} , 10^0 , and 10^2 seconds to monitor temporal changes in V_{th} . This time-resolved approach provided direct insight into the short-term and long-term stability of the programmed states, allowing assessment of the intrinsic drift behavior of the SOM device under realistic operating conditions.

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Supporting Information

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