

Interlayer-Free Ferroelectric Transistors via Depletion Charge Boosting in Oxide Channel for Neuromorphic Applications

Jae Seong Han, Subi Choi, Seok Gyu Hong, Kunho Moon, Ju Hyun Lee, Nam Su Heo, Yoobin Yoon, Sunhee Lee, and Hyun Jae Kim*



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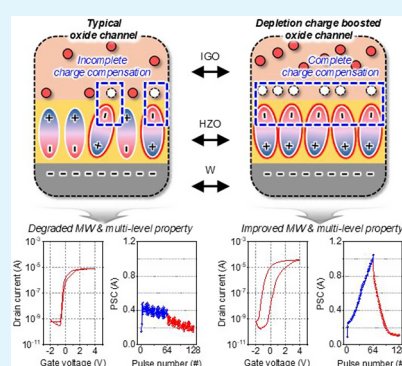
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Supporting Information

ABSTRACT: Oxide semiconductors are considered one of the promising candidates to replace silicon as the channel material in ferroelectric field-effect transistors (FeFETs), owing to their compatibility with low-temperature complementary metal–oxide–semiconductor (CMOS) processing. However, intrinsic hole deficiency in oxide semiconductors limits complete ferroelectric polarization switching, and practical channel engineering strategies to overcome this limitation have rarely been demonstrated. This study demonstrates a depletion charge boosting method via *in situ* Ar⁺ plasma treatment during atomic layer deposition of the indium–gallium oxide (IGO) channel. Under the optimized plasma treatment condition (300 W for 60 s), plasma-induced ionized oxygen vacancies in the IGO front channel function as depletion charges that compensate for the negative bound charges in the zirconium-doped HfO₂ (HZO) layer. The engineered IGO/HZO FeFETs exhibit an improved memory window of 1.612 V, potentiation/depression cycling up to 5120 pulses, and stable multi-level retention of 100 s for 64 conductance states. Furthermore, the multilayer perception-based artificial neural network simulations yield a recognition accuracy of approximately 89% after 125 training epochs. This depletion charge boosting technology provides a potential pathway for improving oxide channel-based FeFETs toward neuromorphic applications.

KEYWORDS: ferroelectric field effect transistors, interlayer-free, depletion charge boosting, charge compensation, zirconium-doped hafnium oxides, indium–gallium oxides



INTRODUCTION

Over the past several decades, the scaling of metal–oxide–semiconductor field-effect transistor (MOSFET)-based devices has been a key strategy for achieving high integration density, fast operating speed, and reduced power consumption.^{1,2} However, further geometric scaling of MOSFET-based devices, which has primarily relied on lateral scaling of channel dimensions and metal pitches, is approaching its physical limits.³ Therefore, fundamentally new concepts and innovations in both computing and hardware are required to sustain further performance improvements.⁴ One approach focuses on overcoming the intrinsic limitation of the conventional von Neumann architecture, such as the memory bottleneck, by adopting neuromorphic computing systems.⁵ These systems can be realized using neuro-inspired transistors capable of exhibiting multi-level conductance states. Such characteristics enable hardware-level integration of memory and computing, thereby reducing system latency and energy consumption.^{6,7} Another approach addresses the limitations of two-dimensional scaling by extending device integration into the vertical dimension through monolithic three-dimensional (M3D) integration. By stacking multiple functional layers with vertical interconnects, M3D integration provides a straightforward and scalable route

to enhance integration density and system-level performance.^{3,4,8} To ensure continued technological advances, the concurrent development of neuromorphic computing architectures and advanced M3D integration is essential. In this context, the realization of M3D-compatible transistors with multiple conductance states is of critical importance.⁹

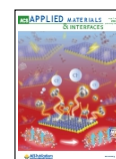
Multi-level memory operation can be implemented using various non-volatile memory (NVM) technologies, such as electrolyte-gated field-effect transistors (EGFETs), floating-gated field-effect transistors (FGFETs), and ferroelectric field-effect transistors (FeFETs).^{6,10–12} Among them, FeFETs based on doped HfO₂ are regarded as one of the most promising candidates, as doped HfO₂ ferroelectric materials offer favorable scalability and compatibility with conventional complementary metal–oxide–semiconductor (CMOS) processes.^{13–16}

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In particular, zirconium-doped HfO_2 (HZO) can be an attractive choice because its ferroelectricity can be realized in a simple binary composition at back-end-of-line (BEOL) compatible temperatures as low as approximately 400 °C.^{17–19} Leveraging these advantages, HZO-based FeFETs have been widely investigated, with early demonstrations predominantly based on MOSFET architectures employing Si channels.^{20–22} However, M3D integration of Si-based devices remains challenging, as Si crystallization requires high annealing temperatures, which can adversely affect the underlying layers.²³ In addition, the formation of defective SiO_2 interfacial layers at the HZO/Si junction can lead to the memory window (MW) narrowing, thereby degrading multi-level memory characteristics.²⁴

From this perspective, oxide semiconductors have emerged as alternatives due to their low temperature processability with conventional CMOS processes, as well as their ability to suppress the formation of undesirable SiO_2 interfacial layers.²⁵ Moreover, oxide semiconductors can be deposited using atomic layer deposition (ALD) technique, which offers excellent step coverage and precise thickness control, making them suitable for M3D integration.^{26–28} Nevertheless, unlike conventional n-type MOSFET-based FeFETs, where holes (accumulation charges) compensate for the polarization charges during erasure, n-type oxide thin-film transistor (TFT)-based FeFETs suffer from incomplete erasure due to the lack of holes (inversion charges) in the channel, as shown in Figure 1a.²⁹ This leads to the MW narrowing, limiting the reliable formation and control of intermediate states between the programmed and erased states, as shown in Figure 1b. To address this issue, previous studies have typically adopted a metal–ferroelectric–metal–insulator–semiconductor (MF MIS) structure, in which the inserted metal layer facilitates polarization switching in the sandwiched ferroelectric layer.^{12,30} However, this approach requires additional processing steps and increases the device footprint to ensure sufficient gate capacitance.³¹ Consequently, channel engineering of ALD-based oxide semiconductors is required for achieving reliable multi-level operation in FeFETs toward M3D integration. However, practical oxide channel engineering strategies to improve multi-level characteristics have rarely been reported, despite the first demonstration of the feasibility of oxide semiconductor-based ferroelectric analog transistors in 2019.³²

This work aims to achieve reliable polarization switching in interlayer-free oxide semiconductor-based FeFETs for enhanced multi-state operation via “depletion charge boosting”. The depletion charges, which correspond to the ionized oxygen vacancies ($V_{\text{O}}^{\bullet}$) in the channel, can compensate for the negative polarization charges in the ferroelectric gate insulator (GI) during the erase operation.^{33,34} A local depletion charge boosting in the oxide semiconductor is realized by adjusting Ar^+ plasma treatment step during the ALD process of the channel. The Ar^+ plasma treatment conditions, including plasma power and treatment time, are optimized through electrical measurements and chemical analyses. In addition, the physical property and spatial distribution of the plasma-induced oxygen vacancies are elucidated via structural and spectroscopic analyses. Based on the optimized treatment conditions, the multi-level operation of depletion charge boosted FeFETs, including endurance and retention characteristics, is evaluated via comprehensive electrical measurements. Finally, artificial neural network (ANN) simulations are performed to assess the feasibility of the proposed depletion charge boosting strategy for FeFET-based neuromorphic computing systems.

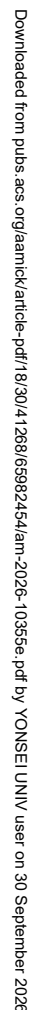
RESULTS AND DISCUSSION

Ferroelectric Property and Channel Engineering in the FeFET

As the oxide semiconductor channel, indium–gallium oxide (IGO) was employed owing to its reliable electrical performance over other oxide semiconductors, which can be effectively tuned by tailoring Ga^{3+} doping concentration.³⁵ We first optimized the Ga_2O_3 ratio in the IGO channel by adjusting the thermal ALD supercycles (see [Experimental Methods](#) for more details.) To evaluate the effect of the Ga_2O_3 ratio, an IGO-based transistor was fabricated using a SiO_2/p^+ -Si substrate serving as the GI/gate, as shown in Figure S1a (Supporting Information). As illustrated in Figure S1b (Supporting Information), the Ga_2O_3 ratio varied from 16.7 to 50.0%, and the transfer characteristics showed that the on/off current ratio was the highest when the Ga_2O_3 ratio was 33.3%. Therefore, an IGO channel with a Ga_2O_3 ratio of 33.3% ($\text{In}_2\text{O}_3:\text{Ga}_2\text{O}_3 = 2:1$) was used throughout this work.

Based on the optimized IGO composition, IGO/HZO FeFETs with a bottom-gate coplanar structure were fabricated, as shown in Figure 2a (see [Experimental Methods](#) for more details.) For the ferroelectric phase transition in the 10 nm-thick HZO layer, a W/HZO/W metal–ferroelectric–metal (MFM) stack was subjected to rapid thermal annealing (RTA) at 400 °C for 30 s under an N_2 ambient.¹⁸ To confirm the ferroelectricity of the HZO layer, polarization–electric field (P–E) hysteresis characteristics were measured using the MFM capacitor with the identical process, as shown in Figure 2b. The P–E loop was obtained by applying a triangular voltage waveform of ± 3 V at 1 kHz. After wake-up cycling of 10^4 cycles, the MFM capacitor exhibited remanent polarization ($2P_r$) of $36.68 \mu\text{C}\cdot\text{cm}^{-2}$, indicating appropriate ferroelectricity. In addition, coercive field ($2E_c$) showed minor variations during the wake-up cycling, as shown in Figure S2 (Supporting Information). This suggests that the wake-up behavior of HZO had a negligible impact on the MW of the FeFETs, since the $2E_c$ is the main factor that determines the MW.³⁶ To confirm the crystalline phase of the ferroelectric HZO, grazing incident X-ray diffraction (GIXRD) measurements were conducted. As shown in Figure 2c, the GIXRD spectra in the 2θ range of $28\text{--}33^\circ$ exhibited a dominant peak at approximately 30.3° . According to the previous reports, the GIXRD peak near 30.5° is attributed to the overlapping (111)o/(011)t reflections, where (111)o corresponds to the noncentrosymmetric ferroelectric orthorhombic phase and (011)t to the centrosymmetric non-ferroelectric tetragonal phase. Considering that the (011)t peak position is shifted to a higher 2θ value relative to the (111)o peak position, the observed peak maximum at 30.3° indicates a higher phase fraction of (111)o phase.^{37,38} Furthermore, the absence of diffraction peaks related to the monoclinic phases indicates a stabilized ferroelectric phase in the HZO. Figure 2d shows the high resolution transmission electron microscope (HR-TEM) image of the ferroelectric HZO region. A well-ordered atomic arrangement of Hf and Zr atoms was observed, with a d -spacing of 2.93 Å, confirming the presence of high-quality ferroelectric phase.

Following the ferroelectric phase transition of the HZO, the IGO channel layer was deposited by thermal ALD using O_3 reactant after patterning a W capping metal to define the source/drain electrodes. Note that [3-(dimethylamino)propyl]-dimethylindium (DADI) and trimethylgallium (TMGa) were



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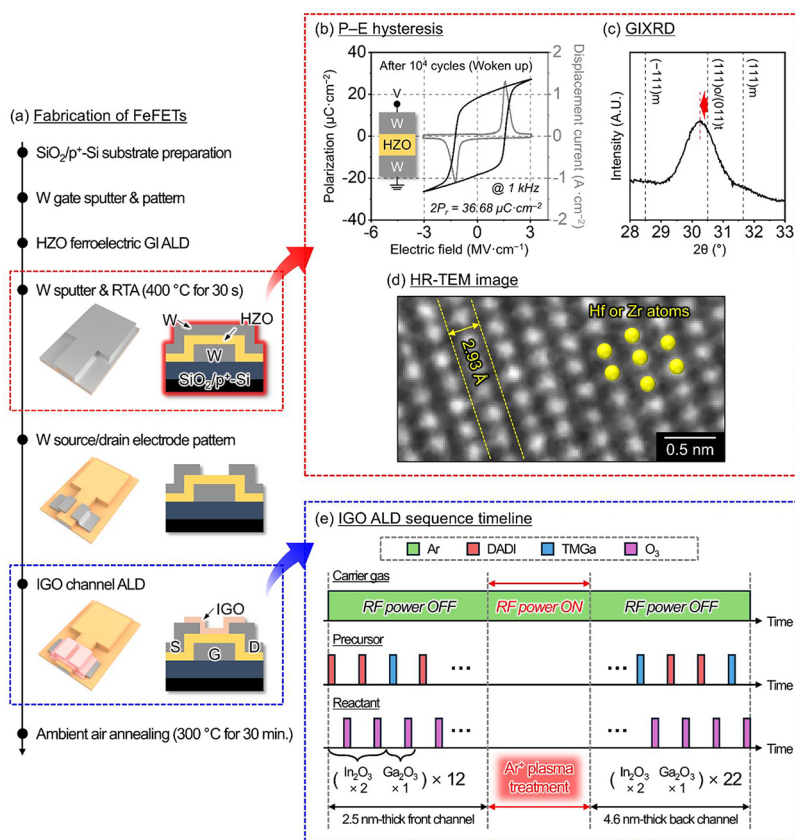


Figure 2. Fabrication process, ferroelectric properties, and channel deposition scheme of the IGO/HZO FeFET. (a) Simplified schematic of the fabrication process of the bottom-gate coplanar-structured IGO/HZO FeFET. (b) Woken-up P–E hysteresis of W/HZO/W MFM capacitors in which the ferroelectric crystallization of HZO was achieved using the same process as that for FeFET fabrication. (c) Corresponding GIXRD spectra for the ferroelectric HZO film. (d) HR-TEM image of the ferroelectric HZO film. (e) Schematic illustration of the ALD sequence timeline for IGO deposition designed for depletion charge boosting.

on-current exhibited a different tendency: it increased up to 300 W but sharply decreased at 400 W. This tendency is summarized in Figure S5 (Supporting Information), where the box plot is based on the five consecutive measurements.

To investigate the effect of Ar^+ plasma power, X-ray reflectivity (XRR) analyses were performed on the IGO front channel region, as the plasma treatment was applied exclusively to this region. Figure 3b presents the spatially resolved-XRR spectra of IGO thin films subjected to various plasma powers in the 2θ range of 0 – 10° . For the non-treated film (0 W), clear interference fringes were observed, and the fitted thickness was approximately 2.32 nm. As the plasma power increased, the fringe intensity gradually diminished, indicating a reduction in film thickness.⁴⁴ In addition, the enlarged XRR spectra in Figure 3c show a steeper decay slope at higher plasma powers, suggesting increased surface roughness, which is likely responsible for the abrupt on-current degradation in transfer characteristics at 400 W.⁴⁵ Figure 3d summarizes the critical angle of XRR spectra for IGO film depending on the plasma power. The critical angle was determined as the point at which the intensity decreases to one-half of the plateau value, as shown in Figure S6 (Supporting Information).⁴⁶ For the non-treated film, the critical angle was approximately 0.75° , whereas the plasma-treated films exhibited relatively lower critical angle values of 0.65° , 0.60° , 0.61° , and 0.58° for 100, 200, 300, and 400 W, respectively. Notably, no significant differences in the critical

angle were observed among the samples treated at 200–400 W. Considering the correlation between the critical angle and film density, these results indicate that the plasma treatment itself decreased the film density; however, the density did not tend to decrease proportionally with increasing plasma power.⁴⁷ According to previous reports, the film density of oxide semiconductors is related to the formation of V_O , and an increase in V_O concentration is generally associated with reduced film density.⁴⁸ Therefore, although Ar^+ plasma treatment promoted the generation of V_O , it is expected that the V_O concentration did not monotonically increase as plasma power increased. This raises the question of why the MW increased with plasma powers. We infer that the MW enhancement could be associated with the proximity of V_O to HZO, rather than the amount of V_O . Generally, ferroelectric polarization can be stabilized by interface or surface charges of the ferroelectric thin film.⁴⁹ Given that the plasma-induced V_O s are predominantly formed at the film surface, the reduction in IGO thickness with increasing plasma power implies closer proximity of the V_O -rich region to the IGO/HZO interface. Accordingly, ionized V_O s generated during erasure are expected to contribute more effectively to charge compensation as the plasma power increases, which is consistent with the tendency observed in the transfer characteristics shown in Figure 3a. However, higher plasma power also increased the surface roughness of the IGO front channel, which could potentially

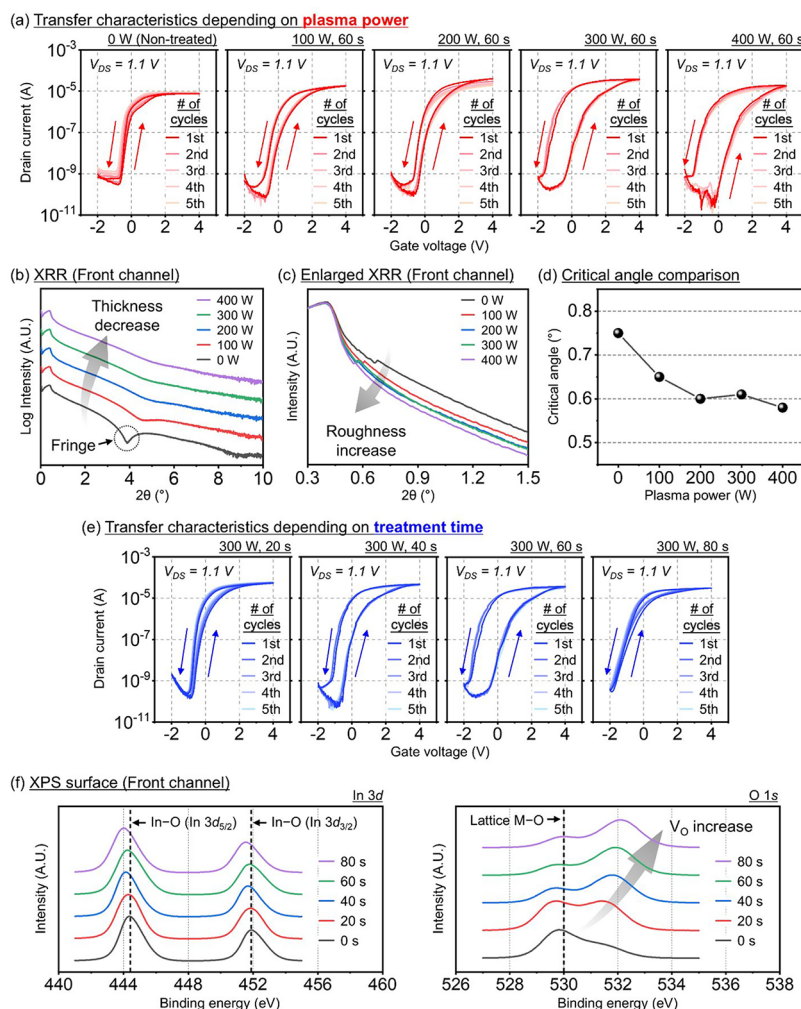


Figure 3. Electrical characteristics and spectroscopic properties of IGO/HZO FeFETs under Ar^+ plasma treatment. (a) Transfer characteristics of IGO/HZO FeFETs depending on Ar^+ plasma power (0, 100, 200, 300, and 400 W). (b) Spatially resolved XRR spectra measured over the 2θ range of 0 – 10° , and (c) enlarged XRR spectra in the 2θ range of 0.3 – 1.5° for the IGO front channel region depending on Ar^+ plasma power. (d) Summarization of the critical angle extracted from the XRR spectra as a function of Ar^+ plasma power. (e) Transfer characteristics of IGO/HZO FeFETs depending on Ar^+ plasma treatment time (0, 20, 40, 60, and 80 s). (f) Spatially resolved XPS spectra of In $3d$ (441–455 eV) and O $1s$ (527–535 eV) depending on Ar^+ plasma treatment time.

induce device reliability issues. Therefore, the optimal condition was determined not solely by the maximum MW alone, but by considering both the MW and the on-current, with 300 W identified as the most favorable condition.

Based on the optimized plasma power condition, the plasma treatment time was varied. Figure 3e shows the transfer characteristics of IGO/HZO FeFETs depending on the Ar^+ plasma treatment time (20, 40, 60, and 80 s), while the plasma power was fixed at 300 W. As shown in Figure S7 (Supporting Information), the gate leakage current remained approximately 10^{-9} A, indicating that the gate leakage had a negligible effect on the hysteresis behavior. As the Ar^+ plasma treatment time increased, the average MW values for five consecutive measurements were 0.264, 0.876, and 1.612 V for 20, 40, and 60 s, respectively; however, the MW became unobservable at 80 s. These trends are summarized in Figure S8 (Supporting Information), where the box plot is based on the five consecutive measurements. To understand this behavior, X-ray photoelectron spectroscopy (XPS) analyses were conducted. Similar to the XRR

analysis, XPS measurements were performed for the IGO front channel region only. As shown in the In $3d$ spectra in Figure 3f, the doublet peaks of In $3d_{5/2}$ and In $3d_{3/2}$, exhibiting an intensity ratio of 3:2, were observed regardless of the plasma treatment time. The binding energies corresponding to the In–O bond are theoretically located at approximately 444.4 eV for In $3d_{5/2}$ and 451.9 eV for In $3d_{3/2}$.⁵⁰ As the plasma treatment time increased, both peaks exhibited a slight shift toward lower binding energy, suggesting an increased contribution from metallic In components.⁵¹ In addition, the O $1s$ spectra shows the main peak near 530.0 eV shifts toward higher binding energy with increasing plasma treatment time. It should be noted that, in the case of XPS surface analysis, compositional analysis based on peak deconvolution may be inaccurate due to contamination from external contaminants such as moisture. Hence, the discussion in this section focuses primarily on peak shifts, while quantitative analysis is presented in the next section.⁵² In oxide semiconductor films, the O $1s$ peak at 530.0 eV is generally attributed to metal–oxide (M–O) bonding, and a positive shift is associated with an

increased fraction of non-lattice components which are closely related to the formation of V_O .⁴² These results indicate that prolonged plasma treatment promotes the generation of V_O in the IGO front channel region. This interpretation is consistent with the monotonic increase in the MW observed in Figure 3e as the plasma treatment time increased up to 60 s. However, further increased generation of V_O at 80 s likely induced a pronounced negative shift in the threshold voltage (V_{TH}), rendering the IGO channel conductive within the operating voltage range, leading to unreadable MW.⁵³ Based on these results, it was confirmed that plasma power influences the relative position at which V_O is generated, whereas plasma treatment time affects the amount of V_O . Accordingly, the optimal condition for depletion charge boosting was determined to be an Ar^+ plasma power of 300 W with a treatment time of 60 s. To confirm the reproducibility of this optimized condition, the device-to-device variation was evaluated, as shown in Figure S9 (Supporting Information). The measured devices exhibited consistent MW, indicating that the optimized plasma treatment condition provides a stable device response.

Finally, the position of the Ar^+ treatment was varied based on the optimized conditions of 300 W and 60 s, as shown in Figure S10 (Supporting Information). When the Ar^+ plasma treatment was performed after the nominal deposition of a 1.3 nm-thick IGO layer, the MW was significantly degraded.

This could be attributed to the formation of oxygen-deficient defects near the IGO/HZO interface, which could narrow the MW via charge trapping. In contrast, when the Ar^+ plasma treatment was applied after the nominal deposition of a 5.0 nm-thick IGO layer, the MW disappeared. In addition, the transfer characteristic appeared similar to that of the non-treated device, indicating the plasma treatment did not have meaningful effect on polarization switching. Therefore, the optimized plasma treatment position was determined to be after the nominal deposition of a 2.5 nm-thick IGO layer.

The structural properties of the IGO/HZO FeFETs with and without Ar^+ plasma treatment were investigated using HR-TEM. Figure 4a presents cross-sectional HR-TEM image of the W/IGO/HZO/W stack for both cases. Each layer was identified based on the energy dispersive spectroscopy (EDS) mapping results shown in Figure S11 (Supporting Information). The top W layer was deposited as a protective layer during focused ion beam (FIB) processing, so no additional annealing was conducted after the deposition of the protective layer. Consistent with the XRR results, the thickness of the IGO channel decreased from 7.1 to 6.2 nm when plasma treatment process was introduced, indicating sputtering of the IGO layer during the plasma process. The HR-TEM images indicate the presence of crystalline phases in the IGO channel,

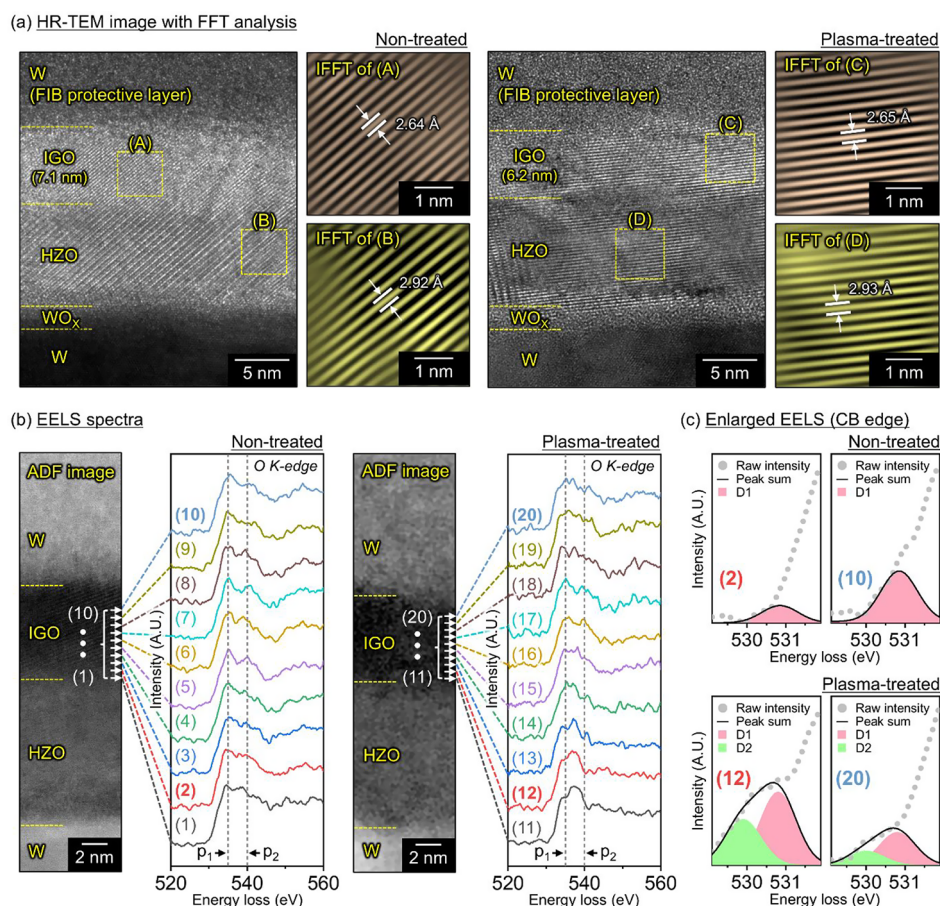


Figure 4. HR-TEM images and EELS spectra. (a) HR-TEM images of non-treated and plasma-treated W/IGO/HZO/W stacks. IFFT images used to confirm crystallinity were obtained from regions (A) and (C) for the IGO channel and (B) and (D) for the HZO GI, respectively. (b) Spatially resolved EELS spectra of non-treated and plasma-treated IGO channels. The positions at which the spectra were acquired are indicated in the corresponding ADF images. (c) Enlarged EELS spectra near the CB edge region. The spectra denoted as (2), (10), (12), and (20) are magnified to compare the CB edge states.

possibly due to annealing in ambient air at 300 °C. A comparison between regions (A) and (C) shows representative *d*-spacings of 2.64 and 2.65 Å, respectively, as determined by inverse fast Fourier transform (IFFT) images. This result suggests that the plasma treatment did not significantly affect the crystallinity of the IGO film. However, the *d*-spacing values were smaller than the representative *d*-spacing of the (222) plane of In₂O₃ (approximately 2.92 Å).²⁶ This reduction could be attributed to the incorporation of Ga into the In₂O₃ lattice, as Ga has smaller atomic radius than In.⁵⁴ Furthermore, crystalline ordering was also observed in the 10 nm-thick HZO layer. The IFFT images of regions (B) and (D) show *d*-spacings of 2.92 and 2.93 Å, respectively, corresponding to the ferroelectric (111) phase of HZO. This is attributed to the thermal stress induced during the RTA process of the W/HZO/W stack.¹⁸

To examine the spatial distribution of V_{O} across the entire IGO channel depending on the Ar⁺ plasma treatment, electron energy loss spectroscopy (EELS) measurements were performed. Figure 4b shows the annular dark field (ADF) images of the W/IGO/HZO/W stack together with the corresponding spatially resolved EELS spectra. The measurement positions of the O K-edge spectra are labeled as (1)–(10) for the non-treated sample and (11)–(20) for the plasma-treated sample in the ADF image. In In₂O₃ and Ga₂O₃ crystals, the O K-edge typically exhibits a doublet peak at approximately 535.0 eV (In 5s and Ga 4s, denoted as p_1), and 540.0 eV (In 5p and Ga 4p, denoted as p_2).^{55,56} In the non-treated sample, the doublet peak was observed across the channel region. The plasma-treated sample on the other hand, showed a noticeable suppression of the doublet peak in the front channel region. In particular, the two peaks appeared partially merged at the positions (11)–(15). In general, merging of the O K-edge doublet peaks in the oxide thin films is attributed to the excessive oxygen incorporation or oxygen deficiency.⁵⁷ Specifically, it is more likely related to the oxygen deficiency considering the results from the XRR and XPS analyses.

To elucidate the nature of this deficiency and examine its spatial distribution, the conduction band (CB) edge region of the O K-edge spectra was analyzed, as shown in Figure 4c. For the non-treated sample, EELS spectra acquired at positions (2) (front channel region) and (10) (back channel region) exhibit a band edge state (denoted as D1) centered at 530.80 ± 0.05 eV. In contrast, the plasma-treated sample, EELS spectra acquired at positions (12) (front channel region) and (20) (back channel region) show not only the D1 component but also an additional state at 529.95 ± 0.05 eV (denoted as D2). Notably, the D2 component was more pronounced in the front channel region. These results indicate that plasma treatment induced additional CB edge states, with a higher concentration near the front channel region. Such band edge states are generally recognized as positively charged donor-like states, suggesting that a fraction of the generated V_{O} s readily existed in ionized states.^{58,59} This interpretation is also supported by the transfer characteristics of the IGO-based transistors with a non-ferroelectric HfO₂ gate insulator with and without plasma treatment, as shown in Figure S12 (Supporting Information). In the plasma-treated device, the on-current increased and more pronounced clockwise hysteresis was observed compared to the non-treated device, indicating that the plasma treatment induced additional mobile carriers, possibly originating from ionized V_{O} s. Consistently, the Hall measurement results for the front channel region show that the plasma-treated front

channel layer exhibited a higher carrier concentration and lower sheet resistance than the non-treated film, as shown in Figure S13 (Supporting Information). Considering that the carrier generation in oxide channels is associated with the formation of the ionized V_{O} s, the Hall measurement results further support the plasma-induced generation of ionized V_{O} s in the front channel region. These ionized V_{O} s are therefore expected to function as depletion charges that compensate for the negative polarization charge in the ferroelectric HZO.

To verify whether ionized V_{O} s are responsible for the MW improvement, the IGO/HZO FeFET with both Ar⁺ plasma treatment and subsequent O₂ plasma treatment was fabricated, as shown in Figure S14a (Supporting Information). Note that the O₂ plasma treatment was also performed in situ within the ALD system, and the plasma power and treatment time were 300 W and 60 s, respectively. As shown in Figure S14b (Supporting Information), both the on-current and MW were severely degraded when the O₂ plasma treatment was applied. This result implies that the generated ionized V_{O} s were compensated by the O₂ plasma treatment, confirming that the ionized V_{O} s play a critical role in improving the device characteristics.

Enhanced Multi-Level Operation and Digit Classification Simulation Based on the Plasma-Treated IGO/HZO FeFETs

Based on the optimized plasma condition, the multi-level characteristics of the IGO/HZO FeFETs with and without plasma treatment were comparatively evaluated. To assess their potential for analog neuromorphic computing, multi-level long term potentiation (LTP) and long term depression (LTD) characteristics were measured. Considering that LTP/LTD properties reflect the gradual adjustment of connection strength between biological synapses, such synaptic characteristics are important for implementing neuromorphic application.⁶⁰ Initially, LTP and LTD characteristics of the plasma-treated device were measured using an identical pulse scheme, as shown in Figure S15a (Supporting Information). However, the resulting synaptic weight update exhibited poor linearity, which is disadvantageous for accurate learning, as shown in Figure S15b (Supporting Information). To ensure learning accuracy, an incremental pulse scheme was used for linear synaptic weight updates.^{32,61,62} As shown in Figure 5a, potentiation pulses were applied from 1.000 to 2.575 V with a step of 0.025 V, while depression pulses were applied from −0.500 to −2.075 V with a step of −0.025 V. As a result, 64 pulses were applied for both potentiation and depression. The pulse width and interval were 50 and 100 ms, respectively. A read pulse of −0.500 V with a duration of 1 ms was used to measure the post synaptic current (PSC). Figure 5b shows the LTP/LTD characteristics depending on plasma treatment. In the non-treated device, PSC exhibited minor variations during pulse application. On the other hand, the plasma-treated device exhibited gradual increases and decreases in PSC during potentiation and depression, respectively. In addition, we examined the device-to-device statistics of the multi-level conductance characteristics using seven devices, as shown in Figure S16 (Supporting Information).

This behavior can be understood based on the schematic mechanism illustrated in Figure 5c, based on the previous electrical measurements and analyses. Plasma treatment partially broke M–O bonding in the front channel region of the IGO lattice, generating additional electrons and ionized V_{O} s. During the program operation, the electrons contribute to the

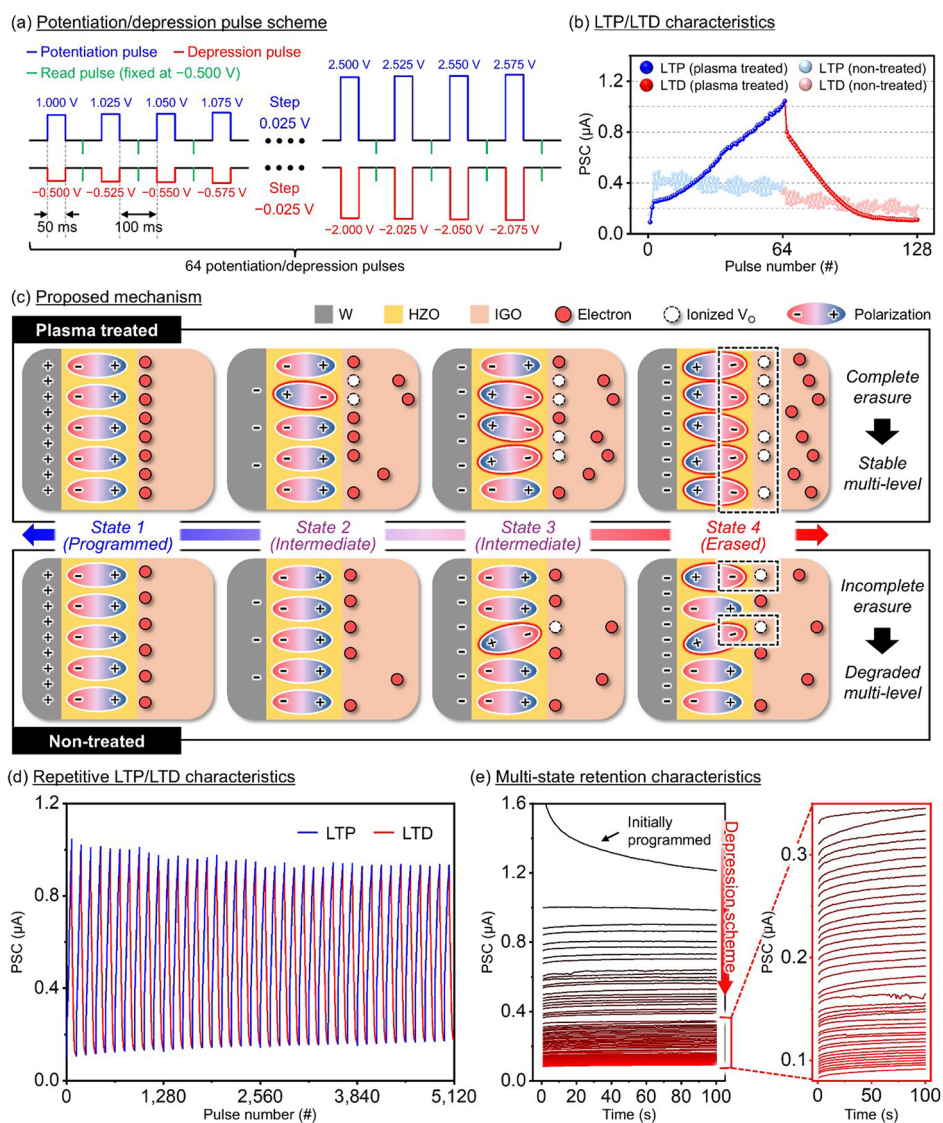


Figure 5. Synaptic properties of the plasma-treated IGO/HZO FeFETs and proposed mechanism. (a) Schematic illustration of the incremental pulse scheme for LTP/LTD evaluation, and (b) corresponding LTP/LTD characteristics for non-treated and plasma-treated IGO/HZO FeFETs. (c) Schematic illustration of the proposed mechanism underlying the enhanced multi-level operation in plasma-treated FeFETs. (d) Repetitive LTP/LTD cycling characteristics and (e) retention characteristics for 64 PSC states.

compensation of positive polarization charges in the HZO. As the device switches to the erase state, electrons are scattered to the back channel region, leaving depletion charges in the front channel. These depletion charges compensate for the negative bound charges, facilitating polarization reversal. Specifically, the extent of polarization reversal is governed by the concentration of depletion charges in the front channel, enabling stable formation of intermediate conductance states. In the non-treated device on the other hand, the insufficient amount of depletion charges that can substitute holes prevents effective polarization reversal in the HZO layer during erasure, resulting in MW disappearance.^{29,63,64} Consequently, the reduced MW limits reliable intermediate state formation, leading to degraded LTP/LTD characteristics. Figure 5d demonstrates repetitive LTP/LTD cycling using 64 consecutive potentiation pulses followed by 64 depression pulses for the plasma-treated IGO/HZO FeFET. After applying a total of

5120 input spike pulses, reliable PSC level modulation was maintained, indicating reliable synaptic weight update under repeated operation. Furthermore, retention characteristics for the 64 states were evaluated via the depression pulse scheme. As shown in Figure 5e, the 64 PSC levels exhibited no obvious degradation after 100 s.

To assess the practical applicability of the plasma-treated FeFET for neuromorphic computing, ANN simulations were conducted. The recognition performance was evaluated using the binarized handwritten image dataset from Modified National Institute of Standards and Technology (MNIST). Figure 6a illustrates the multilayer perceptron (MLP)-based ANN architecture provided by the NeuroSim simulator.⁶⁵ The ANN consisted of 400 input neurons, 100 hidden neurons, and 10 output neurons. The 400 input nodes correspond to the 20 × 20 pixel images derived from the cropped MNIST dataset. Figure 6b shows the pseudo-crossbar array structure

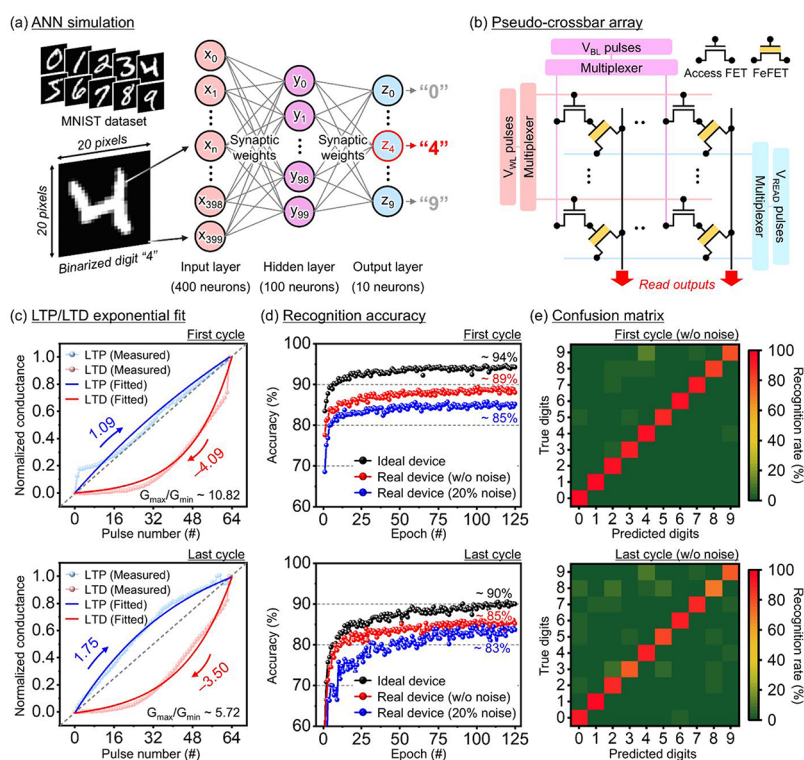


Figure 6. MLP-based ANN simulation results. (a) Schematic illustration of the ANN with three-layered architectures comprising 400 input neurons, 100 hidden neurons, and 10 output neurons. (b) Schematic illustration of the pseudo-crossbar array structure used in the simulation, where a unit cell consists of one access FET and one FeFET. (c) Exponential fitting results of the measured LTP/LTD characteristics for the first and last cycles. (d) Recognition accuracy as a function of training epoch for the ideal device (simulated assuming $NL = 0$ with perfect symmetry) and the real device (simulated with extracted NLs). For the real device, the simulations were performed with and without 20% read noise. (e) Confusion matrices demonstrating classification performance on the MNIST handwritten digit dataset of the real device without read noise.

used in the simulation. Consistent with the FeFET architecture from the NeuroSim simulator, each synaptic cell comprises one access FET and one FeFET. Figure 6c shows the nonlinearity (NL) based on the first and last LTP/LTD cycles for the plasma-treated FeFET. The NL values were extracted from the measured LTP/LTD characteristics using eqs 1–3 with exponential fitting using MATLAB:

$$G_{LTP} = B(1 - e^{-P/A}) + G_{\min} \quad (1)$$

$$G_{LTD} = -B(1 - e^{(P-P_{\max})/A}) + G_{\max} \quad (2)$$

$$B = (G_{\max} - G_{\min}) / (1 - e^{-P_{\max}/A}) \quad (3)$$

Here, G_{LTP} and G_{LTD} denote the conductance values at a given spike pulse number during potentiation and depression, respectively. $G_{\min}$ and $G_{\max}$ represent the minimum and maximum conductance levels, respectively. P indicates the number of applied spike pulse, while $P_{\max}$ corresponds to the total number of pulses required to modulate the conductance from $G_{\min}$ to $G_{\max}$.^{66,67} A is the parameter that characterizes NL, and B is the fitting constant that is expressed as the function of

A . Exponential fitting of the measured conductance update showed the NL of 1.09 for LTP and -4.09 for LTD in the first cycle, and 1.75 for LTP and -3.50 for LTD in the last cycle. Note that the ideal NL value corresponds to 0. The dynamic range, defined as $G_{\max}/G_{\min}$, was 10.82 for the first cycle and 5.72 for the last cycle. Based on these parameters, synaptic weight updates were performed using 60,000 MNIST training images, and the recognition rate was evaluated using 10,000 test images. Figure 6d shows the recognition accuracy as a function of training epoch over 125 epochs. Since read noise can also affect the system performance, ANN simulations for the real device was additionally performed with 20% read noise.^{68–70} Using the first cycle conductance update characteristics, the real device achieved a recognition accuracy of approximately 89%, which is comparable to that of the ideal device with perfectly symmetric LTP/LTD characteristics and $NL = 0$ (approximately 94%). The accuracy remained approximately 85% when applying 20% read noise. Using the last cycle conductance updates, the recognition accuracy of the real device was approximately 85%, while the corresponding ideal device showed approximately 90%. Under 20% read noise, the real device accuracy was maintained at approximately 83%. Figure 6e shows the confusion matrices obtained using the first and last cycle conductance update characteristics without read noise, where the diagonal red components indicate reliable classification of handwritten digits. When 20% read noise was included, the confusion matrices still exhibited pronounced red diagonal components, indicating reliable

classification performance, as shown in Figure S17 (Supporting Information). These results demonstrate the feasibility of the proposed channel engineering strategy for neuromorphic computing applications.

CONCLUSIONS

In this work, we demonstrate a channel engineering technology for IGO/HZO FeFETs by introducing an *in situ* Ar⁺ plasma treatment process during the ALD. Optimization of plasma power and treatment time led to an optimal condition of 300 W for 60 s, achieving a MW of 1.612 V and an on-current of approximately 3×10^{-5} A. Structural and spectroscopic analyses confirmed the formation of localized oxygen deficiency in the front channel region by plasma treatment, and further examination of CB edge states verified that these deficiencies correspond to ionized V_{O} s. The ionized V_{O} s formed in the front channel of crystalline IGO acted as depletion charges that compensate for the negative polarization bound charges of HZO during erasure, thereby enabling reliable polarization switching. This resulted in enhanced multi-level operation characteristics, including stable LTP/LTD cycling over 5120 pulses and retention of 64 conductance states for 100 s. Using experimentally extracted NL and dynamic range values, ANN simulations were performed to evaluate practical applicability for neuromorphic computing. The device showed approximately 89% recognition accuracy on the MNIST dataset, which was comparable to that for the ideal device. These results suggest that depletion charge boosting through plasma-assisted channel engineering could provide potential approach toward M3D-compatible analog FeFETs for neuromorphic applications.

EXPERIMENTAL METHODS

Fabrication of the FeFETs

As the bottom gate electrode, 50 nm-thick W was deposited on a 120 nm-thick thermal SiO₂/p⁺-Si substrate by RF sputtering. The bottom gate was patterned via photolithography followed by wet chemical etching. Standard clean-1 (SC-1) solution (NH₄OH:H₂O₂:H₂O = 1:2:5) was used as the W etchant. The samples were subsequently cleaned with acetone, methanol, and deionized water to prevent any contamination prior to GI deposition. A 10 nm-thick HZO layer was deposited as the ferroelectric GI using thermal ALD method. The detailed HZO ALD process is described in our previous report.³⁴ For the ferroelectric phase transition, a 50 nm-thick W capping layer was deposited on the HZO, followed by RTA at 400 °C for 30 s under N₂ atmosphere. The W capping layer was then patterned using the same photolithography and etching process as the gate electrode to define the source/drain electrodes. The resulting channel width and length were 100 and 10 μm, respectively. The IGO channel was deposited by thermal ALD using DADI, TMGa and O₃ as the indium precursor, gallium precursor, and oxidant, respectively. The growth per cycle values for In₂O₃ and Ga₂O₃ were approximately 0.7 Å/cycle. To optimize the In₂O₃:Ga₂O₃ ratio, the supercycle ratio was varied from 1:1 to 1:5, and the supercycles were repeated until a theoretical thickness of 7.1 nm was achieved. The optimal composition was identified as In₂O₃:Ga₂O₃ = 1:2. Based on this condition, 12 supercycles were first deposited to form the front channel, followed by *in situ* Ar⁺ plasma treatment within the ALD chamber. Subsequently, an additional 22 supercycles were deposited to form the back channel. For comparison, the Ar⁺ plasma treatment conditions were varied, with RF power ranging from 0 to 400 W (0, 100, 200, 300, and 400 W) and treatment time ranging from 0 to 80 s (0, 20, 40, 60, and 80 s). After IGO

deposition, the channel region was defined by photolithography and wet chemical etching using an HCl:H₂O = 1:10 solution. Finally, the devices were annealed in ambient air at 300 °C for 30 min to improve the film quality.

Fabrication of the MFM Capacitors

The W/HZO/W stack was deposited on a 120 nm-thick thermal SiO₂/p⁺-Si substrate, using the same method as the FeFET fabrication. Note that the bottom W electrode was not patterned. Then, the sample was subjected to RTA at 400 °C for 30 s under N₂ atmosphere, for ferroelectric phase transition. Finally, the top W capping layer was patterned via photolithography and wet etching, for top contact electrode formation.

Measurement and Characterization

The electrical measurements of the MFM capacitors and FeFETs were conducted using a semiconductor parameter analyzer (4200A, Keithley Instruments, USA) at room temperature under dark conditions. To confirm the ferroelectric phase of the HZO layer, XRD (SmartLab, Rigaku, Japan) measurements were performed after completely removing the top W capping layer following the RTA process. XRR (SmartLab, Rigaku, Japan) and XPS surface (K-alpha, Thermo Fisher Scientific, U.K.) measurements were conducted to investigate the influence of plasma treatment on the IGO films. The structural and elemental analyses in the IGO/HZO stacks were performed using HR-TEM (Titan 80-300, FEI Company, USA) equipped with EDS mapping and EELS system. Cross-sectional HR-TEM specimens were prepared by an FIB (Crossbeam 350, ZEISS, Germany) milling process. The Hall mobility and sheet resistance of the IGO films were measured using a Hall effect measurement system (HMS-3000, ECOPIA, Republic of Korea).

ANN Simulation

MLP-based ANN simulations were performed using the open-source NeuroSim V3.0 simulator developed by Prof. Shimeng Yu's research team.⁶⁵ The extracted NL and dynamic range parameters, along with the applied pulse scheme, were incorporated into the simulation code. NL extraction was carried out using MATLAB R2024b (MathWorks, Natick, MA, USA), and the recognition accuracy simulations were executed on a Linux-based Ubuntu 22.04 (Canonical Ltd., London, U.K.).

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at <https://pubs.acs.org/doi/10.1021/acsami.6c10355>.

Schematic illustration of the fabrication process and corresponding transfer characteristics depending on IGO supercycle design for IGO-based TFTs; evolution of P-E characteristics of W/HZO/HZO ferroelectric capacitors depending on the wake-up cycles; top-view optical image of the fabricated IGO/HZO FeFET device; gate leakage characteristics of IGO/HZO FeFETs depending on Ar⁺ plasma power (0, 100, 200, 300, and 400 W); summarization of MW and on-current depending on Ar⁺ plasma power (0, 100, 200, 300, and 400 W); the XRR spectra plotted in logarithmic and linear scale within the 2θ range of 0–1° for critical angle determination; gate leakage characteristics of IGO/HZO FeFETs depending on Ar⁺ plasma treatment time (20, 40, 60, and 80 s); summarization of MW and on-current depending on Ar⁺ plasma treatment time (0, 20, 40, 60, and 80 s); statistics of the transfer characteristics of 8 plasma-treated IGO/HZO FeFETs; transfer

characteristics depending on plasma treatment location (nominal 1.3, 2.5, and 5.0 nm-thick IGO); EDS elemental mapping results for non-treated and plasma treated W/IGO/HZO/W stacks; transfer characteristics of IGO/HfO₂ transistors with and without plasma treatment; Hall measurement results of the 2.5 nm-thick IGO front channel with and without plasma treatment; transfer characteristics of IGO/HZO FeFETs with and without oxygen recovery treatment; schematic illustration of the identical pulse scheme for long term potentiation (LTP)/long term depression (LTD) evaluation, and corresponding LTP/LTD characteristics of plasma-treated IGO/HZO FeFETs; statistical characteristics of LTP and LTD characteristics of 7 devices; and confusion matrices demonstrating classification performance on the MNIST handwritten digit dataset for the real device with 20% read noise (DOCX)

AUTHOR INFORMATION

Corresponding Author

Hyun Jae Kim – School of Electrical and Electronic Engineering, Yonsei University, 50, Yonsei-ro, Seodaemun-gu, Seoul 03722, Republic of Korea;  orcid.org/0000-0002-6879-9256; Email: hjk3@yonsei.ac.kr

Authors

Jae Seong Han – School of Electrical and Electronic Engineering, Yonsei University, 50, Yonsei-ro, Seodaemun-gu, Seoul 03722, Republic of Korea

Subi Choi – School of Electrical and Electronic Engineering, Yonsei University, 50, Yonsei-ro, Seodaemun-gu, Seoul 03722, Republic of Korea

Seok Gyu Hong – School of Electrical and Electronic Engineering, Yonsei University, 50, Yonsei-ro, Seodaemun-gu, Seoul 03722, Republic of Korea

Kunho Moon – School of Electrical and Electronic Engineering, Yonsei University, 50, Yonsei-ro, Seodaemun-gu, Seoul 03722, Republic of Korea

Ju Hyun Lee – School of Electrical and Electronic Engineering, Yonsei University, 50, Yonsei-ro, Seodaemun-gu, Seoul 03722, Republic of Korea

Nam Su Heo – School of Electrical and Electronic Engineering, Yonsei University, 50, Yonsei-ro, Seodaemun-gu, Seoul 03722, Republic of Korea

Yoobin Yoon – School of Electrical and Electronic Engineering, Yonsei University, 50, Yonsei-ro, Seodaemun-gu, Seoul 03722, Republic of Korea

Sunhee Lee – Display Research Center, Samsung Display Co., Ltd., 1, Samsung-ro, Giheung-gu, Yongin-si, Gyeonggi-do 17113, Republic of Korea

Complete contact information is available at:

<https://pubs.acs.org/doi/10.1021/acsami.6c10355>

Author Contributions

All authors contributed to the preparation of this manuscript. J.S.H. led and conducted the overall tasks, including device fabrication, electrical measurements, data analysis and interpretation, manuscript writing and editing. S.C. contributed with designing and conducting experiments, as well as data visualization. S.G.H. and K.M. contributed to the electrical

measurements for multi-level operation and ANN simulation. J.H.L., N.S.H., and Y.Y. contributed to the optimization of the device fabrication process. S.L. provided financial support for this work. H.J.K. supervised the overall project. All authors reviewed and approved the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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REFERENCES

- (1) Peercy, P. S. The Drive to Miniaturization. *Nature* **2000**, *406*, 1023–1026.
- (2) Moore, G. E. Cramming More Components onto Integrated Circuits. *Proc. IEEE* **1998**, *86* (1), 82–85.
- (3) Salahuddin, S.; Ni, K.; Datta, S. The Era of Hyper-Scaling in Electronics. *Nat. Electron.* **2018**, *1*, 442–450.
- (4) Liu, X.; Wang, F.; Su, J.; Zhou, Y.; Ramakrishna, S. Bio-Inspired 3D Artificial Neuromorphic Circuits. *Adv. Funct. Mater.* **2022**, *32* (22), 2113050.
- (5) Indiveri, G.; Liu, S.-C. Memory and Information Processing in Neuromorphic Systems. *Proc. IEEE* **2015**, *103* (8), 1379–1397.
- (6) He, K.; Wang, C.; He, Y.; Su, J.; Chen, X. Artificial Neuron Devices. *Chem. Rev.* **2023**, *123* (23), 13796–13865.
- (7) Hong, S.; Cho, H.; Kang, B. H.; Park, K.; Akinwande, D.; Kim, H. J.; Kim, S. Neuromorphic Active Pixel Image Sensor Array for Visual Memory. *ACS Nano* **2021**, *15* (9), 15362–15370.
- (8) Lim, E.; Park, Y.; Youn, C.; Kim, S. Vertical Ferroelectric Capacitors with Excellent Scalability. *Nano Lett.* **2025**, *25* (6), 2166–2172.
- (9) Lee, J.-W.; Park, S.-O.; Yun, S.-Y.; Myung, H.; Choi, S.; Choi, Y.-K. Decoupling Strategy to Separate Training and Inference with Three-Dimensional Neuromorphic Hardware Composed of Neurons and Hybrid Synapses. *ACS Nano* **2025**, *19* (13), 13063–13072.
- (10) Kim, S.-H.; Jin, D.-G.; Kim, J.-H.; Baek, D.; Kim, H.-J.; Yu, H.-Y. Enhancement of the Proton–Electron Coupling Effect by an Ionic Oxide-Based Proton Reservoir for High-Performance Artificial Synaptic Transistors. *ACS Nano* **2025**, *19* (1), 535–545.
- (11) Park, J.; Yun, Y.; Bae, S.; Jang, Y.; Shin, S.; Lee, S.-Y. High-Performance Synapse Arrays for Neuromorphic Computing via Floating Gate-Engineered IGZO Synaptic Transistors. *Adv. Sci.* **2025**, *12* (21), 250068.
- (12) Chen, J.; Li, J.; Zhang, Q.; Xiong, S. High-Performance Ferroelectric Field-Effect Transistors Based on Ultrathin Indium Oxide for Neuromorphic Computing. *ACS Nano* **2025**, *19* (21), 19706–19714.
- (13) Böske, T. S.; Müller, J.; Bräuhäus, D.; Schröder, U.; Böttger, U. Ferroelectricity in Hafnium Oxide Thin Films. *Appl. Phys. Lett.* **2011**, *99*, 102903.
- (14) Müller, J.; Schröder, U.; Böske, T. S.; Müller, I.; Böttger, U.; Wilde, L.; Sundqvist, J.; Lemberger, M.; Kücher, P.; Mikolajick, T.; Frey, L. Ferroelectricity in Yttrium-Doped Hafnium Oxide. *J. Appl. Phys.* **2011**, *110*, 114113.
- (15) Müller, S.; Müller, J.; Singh, A.; Riedel, S.; Sundqvist, J.; Schröder, U.; Mikolajick, T. Incipient Ferroelectricity in Al-Doped HfO₂ Thin Films. *Adv. Funct. Mater.* **2012**, *22* (11), 2412–2417.
- (16) Schröder, U.; Richter, C.; Park, M. H.; Schenk, T.; Pešić, M.; Hoffmann, M.; Fengler, F. P. G.; Pohl, D.; Rellinghaus, B.; Zhou, C.; Chung, C.-C.; Jones, J. L.; Mikolajick, T. Lanthanum-Doped Hafnium Oxide: A Robust Ferroelectric Material. *Inorg. Chem.* **2018**, *57* (5), 2752–2765.

- (17) Müller, J.; Böske, T. S.; Schröder, U.; Müller, S.; Bräuhäus, D.; Böttger, U.; Frey, L.; Mikolajick, T. Ferroelectricity in Simple Binary ZrO_2 and HfO_2 . *Nano Lett.* **2012**, *12* (8), 4318–4323.
- (18) Kim, S. J.; Narayan, D.; Lee, J.-G.; Mohan, J.; Lee, J. S.; Lee, J.; Kim, H. S.; Byun, Y.-C.; Lucero, A. T.; Young, C. D.; Summerfelt, S. R.; San, T.; Colombo, L.; Kim, J. Large Ferroelectric Polarization of $\text{TiN}/\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2/\text{TiN}$ Capacitors Due to Stress-Induced Crystallization at Low Thermal Budget. *Appl. Phys. Lett.* **2017**, *111*, 242901.
- (19) Kim, S. J.; Mohan, J.; Summerfelt, S. R.; Kim, J. Ferroelectric $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ Thin Films: A Review of Recent Advances. *JOM* **2019**, *71*, 246–255.
- (20) Jerry, M.; Chen, P.-Y.; Zhang, J.; Sharma, P.; Ni, K.; Yu, S.; Datta, S. Ferroelectric FET analog synapse for acceleration of deep neural network training, In International Electron Devices Meeting (IEDM), San Francisco, CA, USA, **2017**; pp 6.2.1–6.2.4.
- (21) Seo, M.; Kang, M.-H.; Jeong, S.-B.; Bae, H.; Hur, J.; Jang, B. C. First Demonstration of a Logic-Process Compatible Junctionless Ferroelectric FinFET Synapse for Neuromorphic Applications. *IEEE Electron Device Lett.* **2018**, *39* (9), 1445–1448.
- (22) Khan, A. I.; Keshavarzi, A.; Datta, S. The Future of Ferroelectric Field-Effect Transistor Technology. *Nat. Electron.* **2020**, *3* (10), 588–597.
- (23) Kim, T.; Choi, C. H.; Hur, J. S.; Ha, D.; Kuh, B. J.; Kim, Y.; Cho, M. H.; Kim, S.; Jeong, J. K. Progress, Challenges, and Opportunities in Oxide Semiconductor Devices: A Key Building Block for Applications Ranging from Display Backplanes to 3D Integrated Semiconductor Chips. *Adv. Mater.* **2022**, *35* (43), 2204663.
- (24) Kim, M.-K.; Kim, L.-J.; Lee, J.-S. CMOS-Compatible Ferroelectric NAND Flash Memory for High-Density, Low-Power, and High-Speed Three-Dimensional Memory. *Sci. Adv.* **2021**, *7* (3), eabe1341.
- (25) Park, J. W.; Kang, B. H.; Kim, H. J. A Review of Low-Temperature Solution-Processed Metal Oxide Thin-Film Transistors for Flexible Electronics. *Adv. Funct. Mater.* **2020**, *30* (20), 1904632.
- (26) Kim, D.-G.; Oh, H.-J.; Yang, H. L.; Kho, J.; Kim, Y.; Kuh, B. J.; Park, J.-S. Thermally Stable Crystalline InGaO Channels via Optimized ALD for Advanced DRAM Applications. *ACS Appl. Electron. Mater.* **2025**, *7* (11), 5304–5315.
- (27) Jang, S. C.; Shim, J.; Jang, H.; Lee, Y.; Biswas, S.; Park, J.; Shin, H.; Kim, H.; Kim, S.; Kim, H.-S. Recent Progress in the Development of Backplane Thin-Film Transistors for Information Displays. *J. Inf. Disp.* **2025**, *26* (4), 341–356.
- (28) Hur, J. S.; Jeong, J. H.; Kim, G.-B.; Yoon, S. H.; Koh, J.; Kuh, B. J.; Jeong, J. K. Design of an Atomic Layer-Deposited $\text{In}_2\text{O}_3/\text{Ga}_2\text{O}_3$ Channel Structure for High-Performance Thin-Film Transistors. *ACS Appl. Mater. Interfaces* **2025**, *17* (4), 6541–6549.
- (29) Lee, J. H.; Lee, Y.; Han, J.-K.; Kim, K. D.; Byun, S. R.; Park, H. W.; Hwang, C. S. Gate Engineering Effect in Ferroelectric Field-Effect Transistors with Al-Doped HfO_2 Thin Film and Amorphous Indium-Gallium-Zinc-Oxide Channel. *Adv. Electron. Mater.* **2025**, *11* (3), 2400516.
- (30) Kim, G.; Seok, H.; Son, S.; Choi, H.; Kim, H.; Lee, J.; Kim, G.; Lee, D.; Son, S.; Kim, T. Thermal Expansion-Engineered Ferroelectric Transistor Arrays for Scalable Edge AI Computing. *ACS Nano* **2026**, *20* (5), 4057–4067.
- (31) Wang, X.; Zheng, Z.; Kong, Q.; Jiao, L.; Han, K.; Sun, C.; Zhou, Z.; Liu, L.; Kang, Y.; Liu, G.; Zhang, D.; Gong, X. First Demonstration of BEOL-Compatible MFIS Fe-FETs with 3D Multi-Fin Floating Gate: In-situ ALD-deposited MFIS, LCH of 50 nm, $>2 \times 10^9$ Endurance, and 58.3% Area Saving. In 2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Kyoto, Japan, **2023**; pp 1–2.
- (32) Lee, M.-K.; Lee, J.-S. Ferroelectric Analog Synaptic Transistors. *Nano Lett.* **2019**, *19* (3), 2044–2050.
- (33) Yang, H.; Kim, H.; Kim, H. J.; Kim, D. M.; Choi, S.-J.; Kim, D. H.; Lee, Y. J.; Bae, J.-H. Defect-Mediated Enhancement of Memory Window in IGZO-Channel Ferroelectric Field Effect Transistors. *Mater. Sci. Semicond. Process.* **2026**, *204*, 110268.
- (34) Han, J. S.; Kwak, K.; Choi, S.; Lee, J. H.; Heo, N. S.; Moon, K.; Kim, H. J. Metal-Induced Oxygen Vacancy Control in $\text{InGaZnO}/\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ Ferroelectric Field-Effect Transistor Arrays for Simultaneous Improvement of Memory Window and Electrical Stability. *ACS Nano* **2026**, *20* (2), 2034–2049.
- (35) Gui, Z.; Zou, K.; Xu, M.; Chen, L.; Peng, C.; Li, X.; Zhang, J. High Mobility and Excellent Stability of Solution-Processed Heterojunction-Channel IGO/AIGO TFT. *ACS Appl. Electron. Mater.* **2025**, *7* (8), 3372–3381.
- (36) Ali, T.; Kühnel, K.; Czernohorsky, M.; Rudolph, M.; Pätzold, B.; Olivo, R.; Lehninger, D.; Mertens, K.; Müller, F.; Lerderer, M.; Hoffmann, R.; Mart, C.; Kalkani, M. N.; Steinke, P.; Kämpfe, T.; Müller, J.; Van Houdt, J.; Seidel, K.; Eng, L. M. Impact of Ferroelectric Wakeup on Reliability of Laminate Based Si-doped Hafnium Oxide (HSO) FeFET Memory Cells. In 2020 IEEE International Reliability Physics Symposium (IRPS), Dallas, TX, USA, **2020**; pp 1–9.
- (37) Park, M. H.; Kim, H. J.; Kim, Y. J.; Lee, W.; Moon, T.; Hwang, C. S. Evolution of Phases and Ferroelectric Properties of thin $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ Films According to the Thickness and Annealing Temperature. *Appl. Phys. Lett.* **2013**, *102*, 242905.
- (38) Mehmood, F.; Hoffmann, M.; Lomenzo, P. D.; Richter, C.; Materano, M.; Mikolajick, T.; Schröder, U. Bulk Depolarization Fields as a Major Contributor to the Ferroelectric Reliability Performance in Lanthanum Doped $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ Capacitors. *Adv. Mater. Interfaces* **2019**, *6* (21), 1901180.
- (39) Park, J.-S.; Jeong, J. K.; Mo, Y.-G.; Kim, H. D.; Kim, S.-I. Improvements in the Device Characteristics of Amorphous Indium Gallium Zinc Oxide Thin-Film Transistors by Ar Plasma Treatment. *Appl. Phys. Lett.* **2007**, *90*, 262106.
- (40) Yoo, H.; Kwak, K.; Lee, I. S.; Kim, D.; Park, K.; Kim, M. S.; Han, J. S.; Lee, S.; Kim, T. S.; Lim, J. H.; Kim, H. J. Enhancement of Visible Light Detection for Indium–Gallium–Zinc Oxide-Based Transparent Phototransistor via Application of Porous-Structured Polytetrafluoroethylene. *Appl. Phys. Lett.* **2022**, *121*, 141105.
- (41) Moon, S. J.; Kim, J.-Y.; Kim, J.; Bae, B. S. Photo Response of a-IGZO Thin Films as a Function of Annealing Temperature. *J. Inf. Disp.* **2025**, *26* (4), 461–471.
- (42) Yoon, C. S.; Kim, H. T.; Kim, M. S.; Yoo, H.; Park, J. W.; Choi, D. H.; Kim, D.; Kim, H. J. Vertically Graded Oxygen Deficiency for Improving Electrical Characteristics and Stability of Indium Gallium Zinc Oxide Thin-Film Transistors. *ACS Appl. Mater. Interfaces* **2021**, *13* (3), 4110–4116.
- (43) Cui, T.; Chen, D.; Dong, Y.; Fan, Y.; Yao, Z.; Duan, H.; Liu, J.; Liu, G.; Si, M.; Li, X. Can Interface Layer be Really Free for $\text{HfZr}_{1-x}\text{O}_2$ Based Ferroelectric Field-Effect Transistors With Oxide Semiconductor Channel? *IEEE Electron Device Lett.* **2024**, *45* (3), 368–371.
- (44) Cheema, S. S.; Kwon, D.; Shanker, N.; Reis, R.; dos, Hsu, S.-L.; Xiao, J.; Zhang, H.; Wagner, R.; Datar, A.; McCarter, M. R.; Serrao, C. R.; Yadav, A. K.; Karbasian, G.; Hsu, C.-H.; Tan, A. J.; Wang, L.-C.; Thakare, V.; Zhang, X.; Mehta, A.; Karapetrova, E.; Chopdekar, R. V.; Shafer, P.; Arenholz, E.; Hu, C.; Proksch, R.; Ramesh, R.; Ciston, J.; Salahuddin, S. Enhanced Ferroelectricity in Ultrathin Films Grown Directly on Silicon. *Nature* **2020**, *580*, 478–482.
- (45) Raja, J.; Jang, K.; Nguyen, H. H.; Trinh, T. T.; Choi, W.; Yi, J. Enhancement of Electrical Stability of a-IGZO TFTs by Improving the Surface Morphology and Packing Density of Active Channel. *Curr. Appl. Phys.* **2013**, *13* (1), 246–251.
- (46) Holy, V.; Pietsch, U.; Baumbach, T. *High-Resolution X-Ray Scattering from Thin Films and Multilayers*, Springer Berlin Heidelberg, **1999**. ISBN: 978-3-540-62029-7.
- (47) Bergese, P.; Bontempi, E.; Depero, L. E. A Simple Solution to Systematic Errors in Density Determination by X-ray Reflectivity: The XRR-Density Evaluation (XRR-DE) Method. *Appl. Surf. Sci.* **2006**, *253* (1), 28–32.
- (48) Chowdhury, M. D. H.; Um, J. G.; Jang, J. Remarkable Changes in Interface O Vacancy and Metal–Oxide Bonds in Amorphous Indium–Gallium–Zinc–Oxide Thin-Film Transistors by Long Time Annealing at 250 °C. *Appl. Phys. Lett.* **2014**, *105*, 233504.

- (49) Gattinoni, C.; Strkalj, N.; Härdi, R.; Spaldin, N. A. Interface and Surface Stabilization of the Polarization in Ferroelectric Thin Films. *Proc. Natl. Acad. Sci. U. S. A.* **2020**, *117* (46), 28589–28595.
- (50) Haider, A.; Kizir, S.; Biyikli, N. Low-Temperature Self-Limiting Atomic Layer Deposition of Wurzite InN on Si(100). *AIP Adv.* **2016**, *6*, 045203.
- (51) Henderson, J. D.; Pearson, L.; Nie, H.-Y.; Biesinger, M. C. X-Ray Photoelectron Spectroscopy Analysis of Indium and Indium-Containing Compounds. *Surf. Interface Anal.* **2024**, *57* (1), 81–97.
- (52) Wang, J.; Müller, D. N.; Crumlin, E. J. Recommended Strategies for Quantifying Oxygen Vacancies with X-ray Photoelectron Spectroscopy. *J. Eur. Ceram. Soc.* **2024**, *44* (15), 116709.
- (53) Eom, D.; Kim, H.; Lee, W.; Park, C.; Park, J.; Lee, H.; Kim, T.; Nam, S.; Kim, Y.-H.; Kim, H. Temperature-Driven Co-Optimization of IGZO/HZO Ferroelectric Field-Effect Transistors for Optoelectronic Neuromorphic Computing. *Nano Energy* **2025**, *138* (1), 110837.
- (54) Lee, S. H.; Lee, S.; Jang, S. C.; On, N.; Kim, H.-S.; Jeong, J. K. Mobility Enhancement of Indium–Gallium Oxide via Oxygen Diffusion Induced by a Metal Catalytic Layer. *J. Alloys Compd.* **2021**, *862*, 158009.
- (55) Frati, F.; Hunault, M. O. J. Y.; de Groot, F. M. F. Oxygen K-Edge X-ray Absorption Spectra. *Chem. Rev.* **2020**, *120* (9), 4056–4110.
- (56) Sharma, A.; Varshney, M.; Shin, H.-J.; Chae, K. H.; Won, S. O. Investigation of Cation Distribution and Luminescence in Spinal Phase γ -Ga_{3- δ} O₄:Sm Nanostructures Using X-ray Absorption Spectroscopy. *RSC Adv.* **2017**, *7* (83), 52543–52554.
- (57) Stemmer, S.; Chen, Z. Q.; Zhu, W. J.; Ma, T. P. Electron Energy-Loss Spectroscopy Study of Thin Film Hafnium Aluminates for Novel Gate Dielectrics. *J. Microsc.* **2003**, *210* (1), 74–79.
- (58) Park, H.-W.; Bae, J.; Kang, H.; Kim, D. H.; Jung, P. G.; Park, H. K.; Lee, S. R.; Bae, J. U.; Yoon, S. Y.; Kang, I. P.-3: A Study on the Hot Carrier Effect in InGaZnO Thin Film Transistors. *SID Symp. Dig. Tech. Pap.* **2019**, *50* (1), 1222–1225.
- (59) Yen, C.-C.; Tai, A.-H.; Liu, Y.-C.; Chen, T.-L.; Chou, C.-H.; Liu, C. W. Oxygen-Related Reliability of Amorphous InGaZnO Thin Film Transistors. *IEEE J. Electron Dev. Soc.* **2020**, *8*, 540–544.
- (60) Artola, A.; Singer, W. Long-Term Depression of Excitatory Synaptic Transmissions and Its Relationship to Long-Term Depression. *Trends Neurosci.* **1993**, *16* (11), 480–487.
- (61) Shin, W.; Im, J.; Koo, R.-H.; Kim, J.; Kwon, K.-R.; Kwon, D.; Kim, J.-J.; Lee, J.-H.; Kwon, D. Self-Curable Synaptic Ferroelectric FET Arrays for Neuromorphic Convolutional Neural Network. *Adv. Sci.* **2023**, *10* (15), 2207661.
- (62) Lee, J.; Kim, J.; Kim, M.; Kim, H.; Ra, C.; Choi, H.-W.; Jeon, J. Asymmetry-Aware Compact Modeling of Ferroelectric Devices for Circuit-Level Simulation. *ACS Appl. Electron. Mater.* **2026**, *8* (4), 1614–1625.
- (63) Yoo, S.; Kim, T.; Nam, S.-G.; Kim, D.; Kim, K.; Lee, Y.; Jung, M.; Lee, K.-H.; Choi, S.; Hyun, S. D.; Lee, M.-H.; Hong, S.; Kim, H.; Bae, K. D.; Lee, H.; Won, J. Y.; Yun, D.-J.; Chae, B. G.; Hahn, W. G.; Joo, C. H.; Jo, S.; Park, Y.; Song, K. M.; Jung, K.; Lim, S.; Seo, K.; Kim, K.; Kim, W.; Ha, D.; Yang, J.-E.; Yang, S.-Y.; Kim, S.; Heo, J.; Choe, D.-H. Ferroelectric Transistors for Low-Power NAND Flash Memory. *Nature* **2025**, *648* (8403), 320–326.
- (64) Shen, B.; Yang, B.; Shi, M.; Sun, W.; Liu, H.; Ding, Y.; Gao, B.; Qian, H.; Wang, Y.; Tang, J.; Wu, H. Review on Ferroelectricity and Atomic Characterization of Hf_{0.5}Zr_{0.5}O₂ in FeRAM. *ACS Appl. Electron. Mater.* **2025**, *7* (11), 4675–4702.
- (65) Chen, P.-Y.; Peng, X.; Yu, S. *NeuroSim+: An Integrated Device-to-Algorithm Framework for Benchmarking Synaptic Devices and Array Architectures*. In 2017 International Electron Devices Meeting (IEDM), San Francisco, CA, USA, **2017**; pp 6.1.1–6.1.4.
- (66) Kwak, K.; Park, K.; Han, J. S.; Kang, B. H.; Choi, D. H.; Moon, K.; Hong, S. M.; Kim, G. I.; Lee, J. H.; Kim, H. J. Swiftly Accessible Retinomorphic Hardware for In-Sensor Image Preprocessing and Recognition: IGZO-based Neuro-Inspired Optical Image Sensor Arrays with Metallic Sensitization Island. *Int. J. Extrem. Manuf.* **2025**, *7* (6), 065504.
- (67) Moon, K.; Rho, S. M.; Kim, B.; Kwak, K.; Kim, B. S.; Choi, D. H.; Kang, B. H.; Chung, J. J.; Kim, H. J. Biocompatible Neuromorphic Device Array Based on Naturally Sourced Mucin for Implantable Bioelectronics. *ACS Nano* **2025**, *19* (10), 10400–10411.
- (68) Wu, H.; Lin, Z.; Liu, J.; Zhang, C.; Tan, C.; Wang, Z. Ta₂PdS₆/MoS₂ Heterojunction Phototransistor for High-Performance Photoelectric Synapses and Graphic Identification. *ACS Appl. Mater. Interfaces* **2025**, *17* (13), 20116–20124.
- (69) Tan, C.; Wu, H.; Lin, Z.; Yang, L.; Hu, G.; Wang, Z. In-Plane Polarization Induced Depletion, Photovoltaic and Memory Effects in Ferroelectric Junction Field-Effect Transistor. *Adv. Funct. Mater.* **2026**, *36* (1), e07832.
- (70) Lin, Z.; Wu, H.; Tan, C.; Hu, G.; Wang, Z. Dual-Wavelength Synaptic Simulator ReS₂/Ta₂NiSe₅ for Multi-Timescale Learning in Neuromorphic Computing. *Small* **2025**, e05586.