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Reliability Enhancement of Oxide Thin-Film Transistors via Suppression of a-IGZO Protrusions for Improved Image Quality in LTPO AMOLED Displays

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ABSTRACT

We identify a new origin of oxide thin-film transistor (TFT) instability and propose a process-level approach to effectively overcome reliability-induced degradation in low-temperature polycrystalline silicon and oxide (LTPO) backplanes. Multi-buffer protrusions originate from non-uniform LTPS processes, including excimer laser annealing and subsequent active-layer dry etching. These protrusions are transferred into the subsequently formed oxide TFT stack, inducing protrusion variations in the amorphous indium-gallium-zinc-oxide (a-IGZO) channel. Microscopic structural analyses, along with electrical characterization, demonstrate that these a-IGZO channel protrusion variations lead to threshold-voltage (V_{TH}) variation and mobility degradation in oxide TFTs. To mitigate this issue, the active layer dry-etch process is optimized to enhance the etch selectivity between the polycrystalline silicon and multi-buffer layers. The optimized process reduces multi-buffer protrusion heights from 5.1 to 1.6 nm and improves a-IGZO channel protrusion uniformity within a single panel, thereby decreasing V_{TH} variation after reliability testing from 0.92 to 0.15 V across the panel. This study reveals the root cause of oxide TFT instability and proposes effective process solutions for LTPO active-matrix organic light-emitting diode (AMOLED) displays.

1 | Introduction

Active-matrix organic light-emitting diode (AMOLED) displays have emerged as a key display technology for smartphones, smart-watches, and tablet computers, continuously advancing toward higher power efficiency, superior image quality, and smoother visual performance [1–5]. Low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) have been widely adopted in active-matrix displays due to their high carrier mobility and excellent electrical performance. Low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) have long been the mainstream backplane technology owing to their high carrier

mobility and strong driving capability, enabling high-resolution and high-refresh-rate AMOLED displays [6–10]. However, LTPS TFTs inherently suffer from relatively large leakage currents, which degrade long-term data retention and increase both power consumption and image quality deterioration during extended operation [11–14].

In order to address these limitations, oxide TFTs, represented by amorphous indium gallium zinc oxide (a-IGZO), have attracted considerable attention [15–20]. Owing to their extremely low leakage current, oxide TFTs are well-suited for switching applications and have been extensively investigated for their electrical

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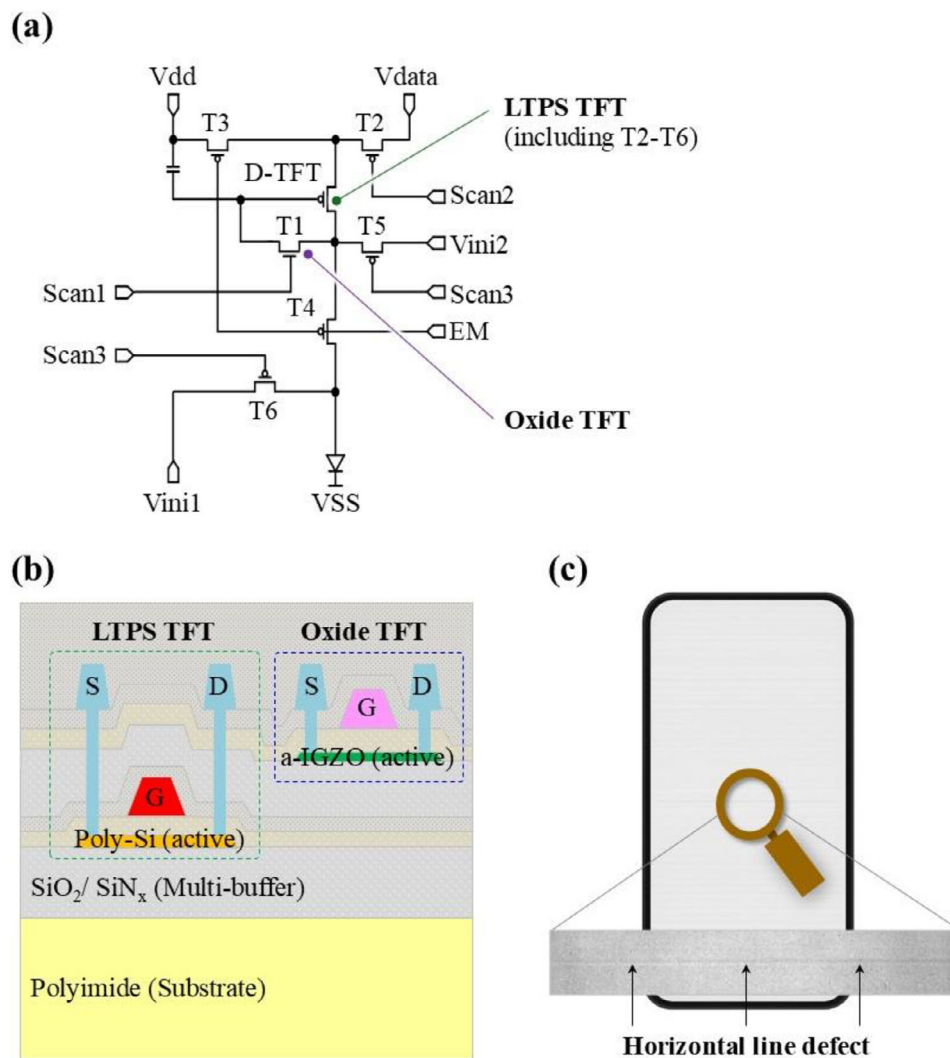


FIGURE 1 | (a) Schematic of an LTPO pixel circuit in which the LTPS TFTs act as the driving and switching transistors, whereas the oxide TFT serves as the switching (sampling) transistor. (b) Corresponding schematic cross-sectional structure of an LTPO panel. (c) Photograph of a horizontal line defect observed after THB reliability testing, exhibiting locally reduced luminance in the defect region.

stability and process compatibility in next-generation backplane technology [21, 22]. However, a-IGZO-based oxide TFTs exhibit intrinsic drawbacks such as relatively low mobility and threshold-voltage (V_{TH}) instability under bias stress, restricting their use in high refresh rate or long operation environments [23–27].

To overcome these challenges, the low-temperature polycrystalline silicon and oxide (LTPO) architecture was introduced to combine and enhance the complementary advantages of LTPS and oxide TFTs [28, 29]. As shown in Figure 1a,b, the LTPO structure consists of LTPS and oxide TFTs fabricated on the same backplane, where the LTPS TFTs serve as driving and switching transistors, and the oxide TFT is used as the switching (sampling) transistor connected to the gate node of the driving transistor. This hybrid structure enables prolonged gate voltage retention for low refresh rate operation while supporting a variable refresh rate (VRR, 1–120 Hz) to improve power efficiency [30–35].

However, despite these advantages, LTPO displays exhibit unexpected image quality degradation under reliability stress. Pre-

vious studies have reported various reliability issues in oxide TFTs, including hydrogen diffusion and V_{TH} variations under bias stress [36–39]. Nevertheless, several reliability problems in oxide TFTs remain unresolved, and their underlying causes have not been clearly identified. In our reliability evaluation using a temperature humidity bias (THB, 60°C, 90% RH, 500 h) test, we observed unexpected image quality degradation in LTPO displays. The THB reliability test was performed at the panel level under dynamic driving conditions rather than under fixed bias stress. During panel operation, the gate voltage of the oxide TFTs typically varied from approximately -10 to $+10$ V depending on the display content and driving frequency. In addition, the driving frequency was varied from 120 to 1 Hz to reflect realistic operating conditions of mobile displays. Before the THB reliability test, the panels were inspected through electrical characterization and optical inspection, and only defect-free panels were used for the reliability test. As shown in Figure S1, no image defects were observed and the oxide TFTs showed typical electrical characteristics before the THB reliability test. However, as shown in Figure 1c, a horizontal line defect with locally reduced luminance

is observed after the THB reliability test. Therefore, to address this issue, it is essential to identify the root causes of oxide TFT characteristic non-uniformity.

In this study, we systematically investigated the causes of reliability-induced image quality degradation in LTPO displays. By combining focused ion beam (FIB), scanning electron microscopy (SEM), and atomic force microscopy (AFM) structural analyses with electrical characterization, we identified the inherent weaknesses of the LTPO architecture and demonstrated that a-IGZO channel protrusion variation directly affects the electrical characteristics of oxide TFTs and the resulting display image quality.

2 | Results and Discussion

2.1 | Structural Origin of a-IGZO Channel Protrusion Variation

We performed detailed FIB, SEM, and AFM structural analyses on oxide TFTs located in both the line defect region (LDR) and the adjacent reference region (RR) within the same panel, where the RR does not exhibit the line defect. The specific measurement locations for the RR and LDR are described in detail in Figure S2. These analyses were conducted to identify the root cause of the horizontal line defect observed after THB reliability testing. Through FIB cross-sectional structural analysis of the RR and LDR, it was found that the oxide TFT in the RR, shown in Figure 2a, maintains a flat and uniform a-IGZO channel. In contrast, the oxide TFT in the LDR, shown in Figure 2b, exhibits severe protrusions formed on the a-IGZO channel. These results reveal that a-IGZO channel protrusion variation exists within a single panel, and that such structural non-uniformity affects the electrical characteristics of oxide TFTs, eventually leading to image quality degradation after reliability stress.

To further investigate the origin of the a-IGZO channel protrusion variation observed in Figure 2b, additional structural analyses were performed on the underlying LTPS TFT. In particular, SEM and AFM measurements were carried out to examine how surface irregularities generated during the LTPS process are transferred into the multi-buffer layer. The SEM and AFM measurement locations corresponding to these analyses are illustrated in detail in Figure S3. Figure 2c presents SEM top-view images of the LDR after the active dry-etch process, captured at progressively higher magnifications for detailed defect analysis. At low magnification (left), the overall structure of the polycrystalline silicon (poly-Si) active layer and multi-buffer can be observed, whereas distinct protrusions on the multi-buffer layer become clearly visible at higher magnification. During LTPS TFT active formation, excimer laser annealing (ELA) crystallizes amorphous silicon (a-Si) into poly-Si, forming grain boundaries, which appear as surface protrusions [40]. Because the multi-buffer layer is not directly exposed to the ELA process, such protrusions should not form in this layer. However, these protrusions are absent in the RR but observed in the LDR.

The corresponding AFM analysis was performed on the multi-buffer surface to quantitatively evaluate these protrusions. As shown in Figure 2d,e, AFM measurements were performed on

multiple horizontal line defect samples ($N = 15$) to obtain a reliable statistical distribution. The resulting height distribution revealed an average protrusion height of approximately 5.1 nm. Given that the total thickness of the multi-buffer stack is about 800 nm approximately a 5 nm protrusion represents a substantial structural deformation. Furthermore, because the a-IGZO channel thickness is typically only 20–30 nm, such a protrusion is sufficiently large to degrade the uniformity and stability of the a-IGZO channel.

Based on the combined FIB, SEM, and AFM structural analyses, the root cause of a-IGZO channel protrusion variation was identified, as illustrated in Figure 3. Figure 3a shows the cross-sectional structure of the poly-Si layer, the $\text{SiO}_2/\text{SiN}_x$ multi-buffer, and the polyimide substrate after ELA crystallization. Grain boundaries formed during ELA on the poly-Si layer and appear as protrusions. Figure 3b shows the surface protrusion of both the poly-Si active layer and the multi-buffer layer after the dry-etch process. Although protrusions should ideally appear only on the top surface of the poly-Si active layer, additional protrusions are observed on the multi-buffer surface due to insufficient etch selectivity during the dry-etch process. Figure 3c shows that these protrusions on the multi-buffer surface are transferred into the upper insulator layers during subsequent processing, forming corresponding protrusions in the upper stack. As shown in Figure 3d, when the oxide TFT is deposited on top of the multi-buffer layer, these transferred protrusions propagate into the oxide TFT layer, resulting in a-IGZO channel protrusion variation within the same panel.

In LTPO, LTPS and oxide TFTs are integrated within the same panel and therefore necessarily share the same layer stack [28]. Because of this shared structure, any non-uniformities originating from the LTPS process are unavoidably propagated into the a-IGZO channel, leading to instability and ultimately manifesting as horizontal line defects and image quality degradation in LTPO displays.

2.2 | Instability of Oxide TFTs Caused by a-IGZO Channel Protrusion

To investigate how structural non-uniformity of a-IGZO channel protrusions affects the electrical properties of oxide TFTs, electrical measurements were conducted. The results demonstrate that a-IGZO channel protrusions induce localized electrical instability within the same panel. A detailed electrical analysis of the oxide TFTs is presented in Figure 4. Figure 4a,b present the transfer characteristics plotted on logarithmic and linear scales to clearly distinguish the subthreshold behavior and the current variation, respectively. The black and red curves represent the devices measured in the RR and LDR. As shown in Figure 4a, the logarithmic scale ($I_{\text{DS}}-V_{\text{GS}}$) exhibits a clear positive shift in V_{TH} in the LDR compared with the RR after THB stress. In addition, the linear-scale ($I_{\text{DS}}-V_{\text{GS}}$) curves in Figure 4b show a noticeable reduction in slope of the LDR curve, indicating mobility degradation. These electrical degradations align well with the results of the structural analysis presented in Section 2.1, confirming that a-IGZO channel protrusion directly leads to instability in oxide TFTs. The statistical box plots ($N = 15$) in Figure 4c,d present the results measured from multiple horizontal

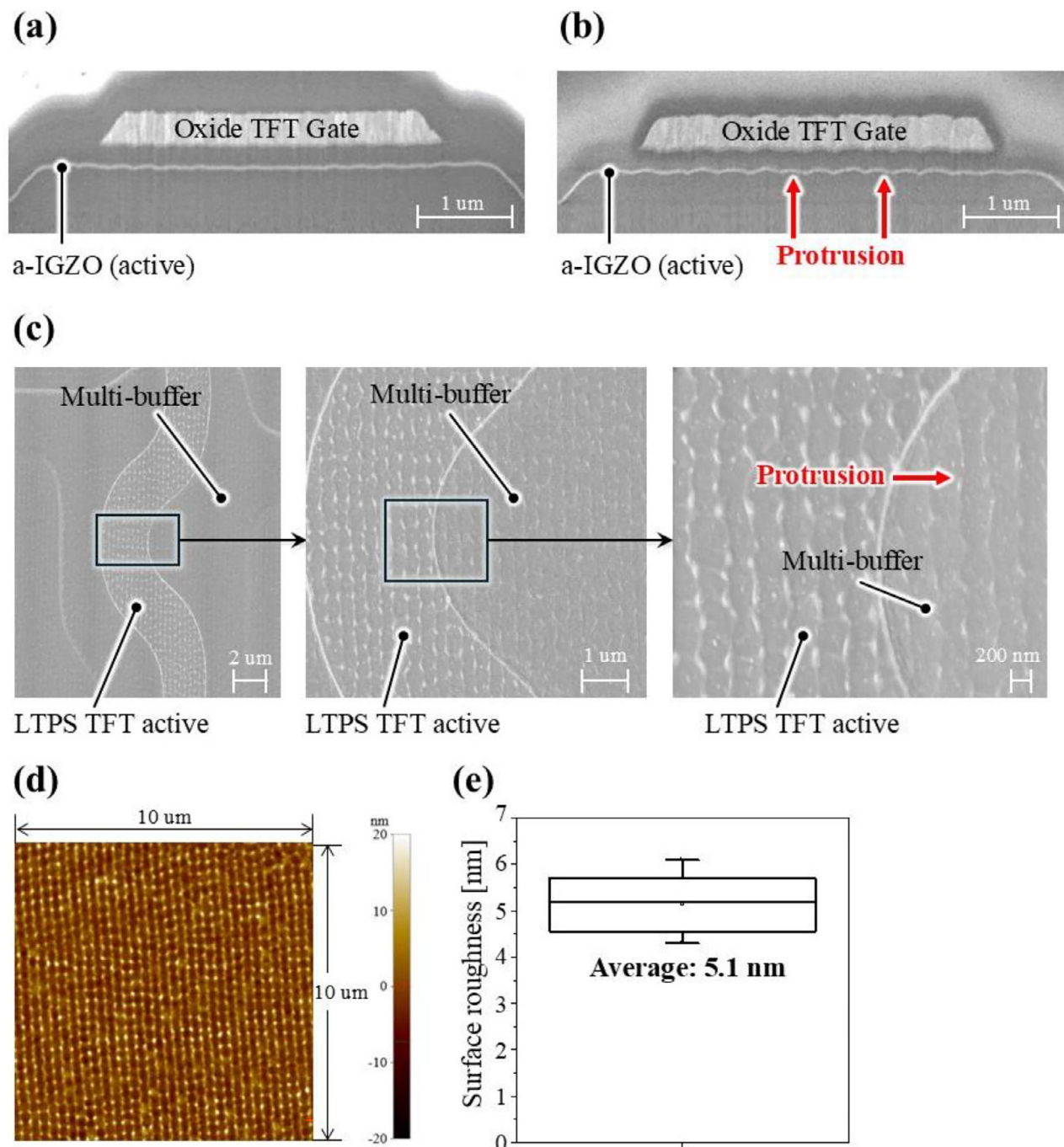


FIGURE 2 | Structural analysis of the LTPO backplane—including the LTPS TFT and oxide TFT layers—in the reference region (RR) and line defect region (LDR). (a) FIB cross-sectional image of the oxide TFT at the RR. (b) FIB cross-sectional image of the oxide TFT at the LDR showing noticeable surface protrusions. (c) SEM top-view image of the LDR after the active dry-etch process, revealing protrusions formed on the multi-buffer layer. (d) AFM image of the LDR showing rough surface protrusion. (e) AFM-based protrusion height distribution obtained from multiple LDRs across horizontal line defect samples, exhibiting an average height of approximately 5.1 nm.

line defect panels to improve the reliability of the analysis. Devices located in the LDR exhibit an average positive V_{TH} shift of approximately 0.92 V and an average mobility degradation of about 17% compared with those in the RR.

The reasons why oxide TFT characteristics vary within the same panel can be explained by two main factors arising from differences in a-IGZO channel protrusion, which are conceptually illustrated in Figure S4. One of them is that a-IGZO

channel protrusion variations can change the effective channel length within the same panel. While the oxide TFT channel length in the RR is formed as designed, the channel in the LDR has a longer effective channel length than the RR due to surface protrusion. To quantitatively verify this effect, the effective channel length was systematically extracted from FIB cross-sectional images at locations above and below the LDR within the same panel, as summarized in Figure S5. The results show that the effective channel length is increased only in the

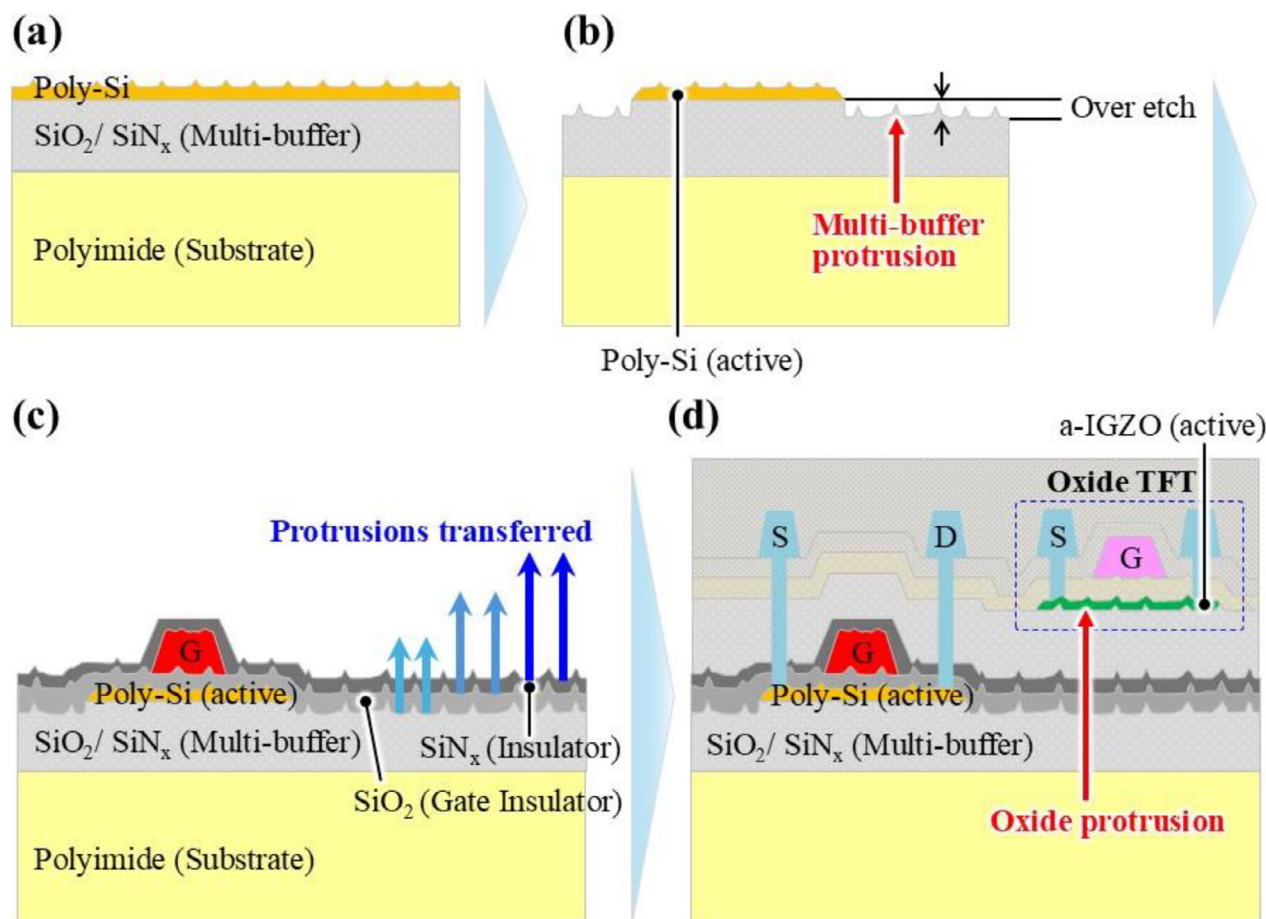


FIGURE 3 | Illustration of the root cause of oxide protrusion variation. (a) Surface protrusions are generated on the poly-Si surface after the ELA crystallization process, where grain boundaries are formed and appear as surface protrusions. (b) After the LTPS TFT active dry-etch process, insufficient dry-etch selectivity between the poly-Si active and multi-buffer layers causes over-etching, producing additional protrusions to form on the multi-buffer surface. (c) The protrusions formed on the multi-buffer surface are transferred into the upper gate-insulator layers during subsequent processing, creating corresponding protrusions in the upper stack. (d) When the oxide TFT is deposited on top of the multi-buffer, these transferred protrusions propagate into the oxide TFT layer, resulting in protrusion formation on the a-IGZO channel.

LDR, whereas the effective channel length in the surrounding RR remains unchanged, indicating that a-IGZO channel protrusions locally increase the effective channel length within the same panel. This difference causes variations in carrier transport efficiency and V_{TH} between the two regions after reliability stress [41, 42]. The other factor is the difference in charge trapping between the two regions. Under THB stress conditions, the rough surface protrusion increases the local electric field concentration, which accelerates electron trapping at the oxide/gate-insulator interface [43, 44]. The roughened surface region tends to trap more electrons at the interface. Compared to the RR, the LDR has a more roughened channel surface, trapping more electrons, which reduces the free charge concentration within the channel and degrades the field-effect mobility. This effect was further examined by repeatedly measuring the capacitance between the a-IGZO active layer and the oxide TFT gate, as shown in Figure S6. Compared with the RR, the LDR exhibits increased capacitance fluctuations. These capacitance fluctuations indicate locally non-uniform electric fields, suggesting that the formation of a-IGZO channel protrusions induces local electric-field non-uniformity and consequently leads to increased charge trapping at the protruded interface. In summary, a-IGZO channel protrusion

variations cause differences in effective channel length and charge trapping, which leads to electrical instability of oxide TFTs within the same panel.

2.3 | Process Optimization for Suppression of a-IGZO Channel Protrusion Variation

The structural and electrical analyses presented above reveal that the horizontal line defects in LTPO displays originate from non-uniform a-IGZO channel protrusions in oxide TFTs. These a-IGZO channel protrusions arise from the transfer of protrusions formed in the multi-buffer layer. Therefore, suppressing protrusion formation in the multi-buffer layer is essential to minimizing a-IGZO channel protrusion variation and reducing reliability-induced failures.

Figure 5 illustrates the origin of multi-buffer protrusion formation and the associated improvement mechanism related to dry-etch selectivity. The formation of multi-buffer protrusions mainly results from insufficient dry-etch selectivity between the poly-Si active layer and the underlying multi-buffer layer. Since the two

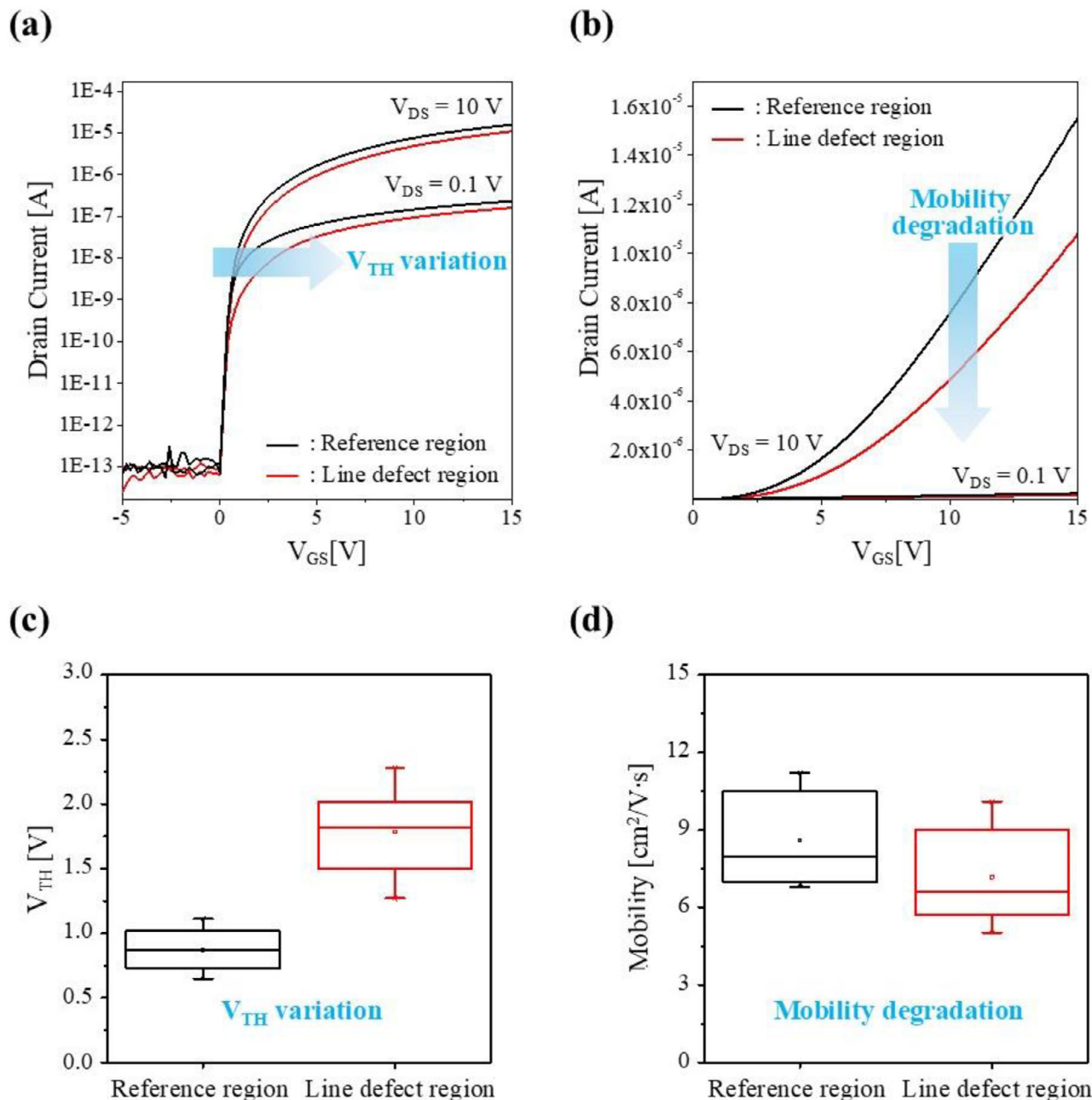


FIGURE 4 | Electrical analysis of oxide TFTs in the RR and LDR after THB stress, showing threshold-voltage variation and mobility degradation. (a) Log-scale (I_D - V_{GS}) transfer characteristics of oxide TFTs measured at the RR and LDR after THB stress, showing a positive V_{TH} shift in the LDR. (b) Linear-scale (I_D - V_{GS}) curves showing reduced drain current in the LDR, indicating mobility degradation. For each region, the upper and lower curves correspond to measurements performed at a high drain bias ($V_{DS} = 10$ V) and a low drain bias ($V_{DS} = 0.1$ V), respectively. (c) Statistical distribution of V_{TH} variation obtained from oxide TFTs measured across multiple horizontal line defect panels ($N = 15$), showing an average shift of approximately 0.92 V in the LDR. (d) Statistical distribution of mobility variation measured across multiple horizontal line defect panels ($N = 15$), exhibiting an average degradation of approximately 17% in the LDR.

layers are composed of different materials, insufficient selectivity causes unintended over-etching of the multi-buffer during the active dry-etch process, leading to buffer loss and the generation of surface protrusions, as shown in Figure 5a. In contrast, as shown in Figure 5b, enhanced selectivity allows the poly-Si active layer to be removed cleanly while minimizing multi-buffer damage, thereby preventing protrusion formation. To experimentally validate this origin, Figure 5c,d shows SEM top-view and FIB cross-sectional images obtained under the conventional

and optimized dry-etch conditions. Under the conventional dry-etch condition shown in Figure 5c, pronounced multi-buffer loss is observed on the surface, which is consistently confirmed in the FIB cross-sections. In contrast, under the optimized etching conditions (Figure 5d), a smooth interface without protrusions is observed, and the FIB cross-sectional images also confirm the absence of multi-buffer loss. Additional high-resolution transmission electron microscopy (TEM) cross-sectional images supporting the multi-buffer loss are provided in Figure S7.

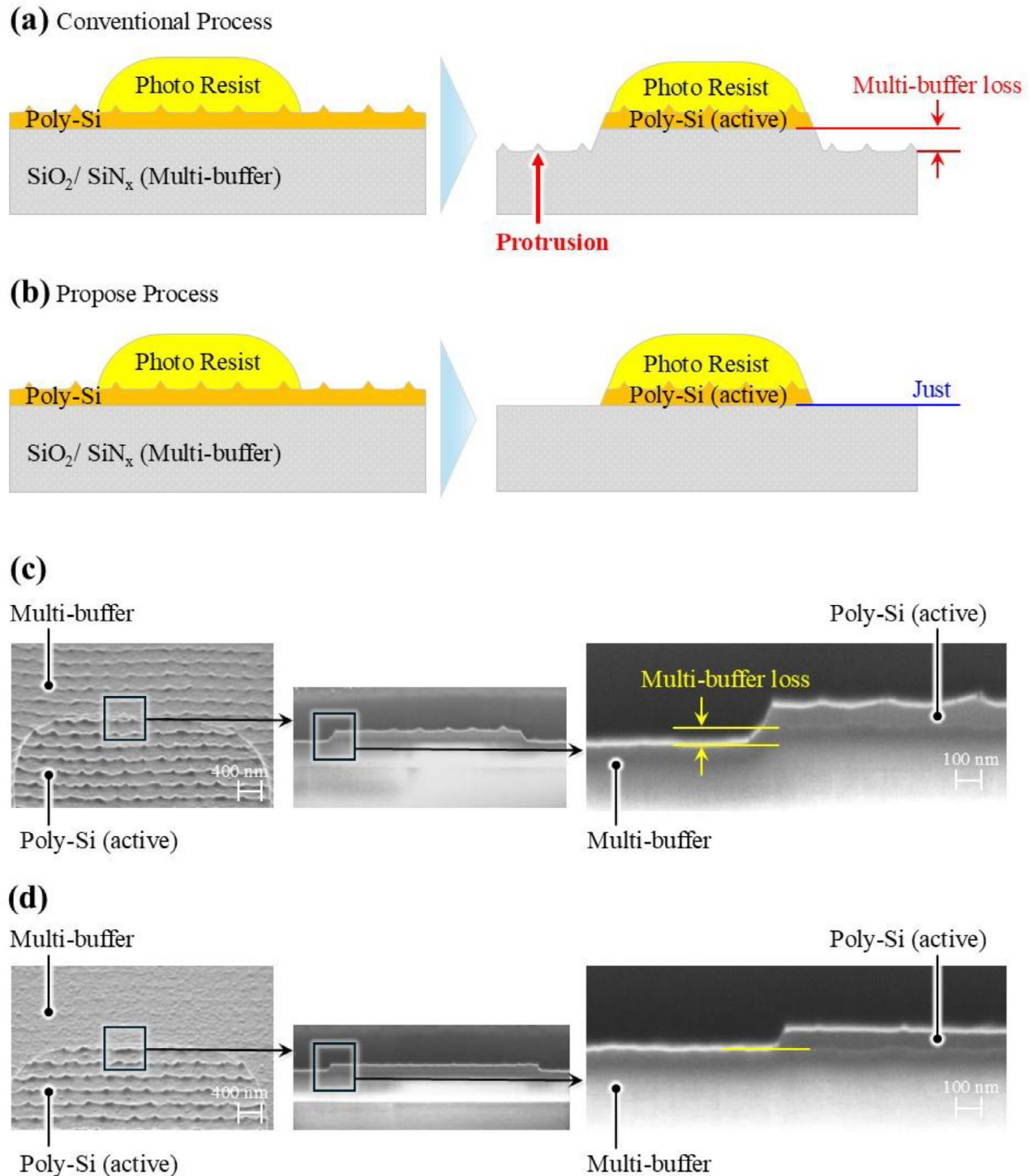


FIGURE 5 | Mechanism and experimental verification of multi-buffer protrusion formation. (a) In the conventional dry-etch process, insufficient etch selectivity between the poly-Si active layer and the underlying multi-buffer layer causes multi-buffer loss and generates surface protrusions. (b) The proposed dry-etch process improves the etch selectivity, effectively suppressing multi-buffer loss and maintaining a planar interface. (c) SEM surface image and corresponding FIB cross-sectional image obtained under the conventional condition, showing severe multi-buffer loss. (d) SEM surface image and FIB cross-sectional image obtained under the optimized condition, demonstrating suppressed multi-buffer loss and a uniform LTPS–multi-buffer interface.

These results clearly indicate that insufficient dry-etch selectivity during the LTPS TFT active-layer process induces severe multi-buffer loss, and that optimization of the dry-etch process is essential to fundamentally improve a-IGZO channel protrusion variation.

Based on these results, a design of experiments (DOE) approach was employed to optimize the dry-etch process by improving the poly-Si/SiO₂ etch selectivity, which was approximately 1:1 under the conventional dry-etch condition and led to multi-buffer loss and protrusion formation. As summarized in Table

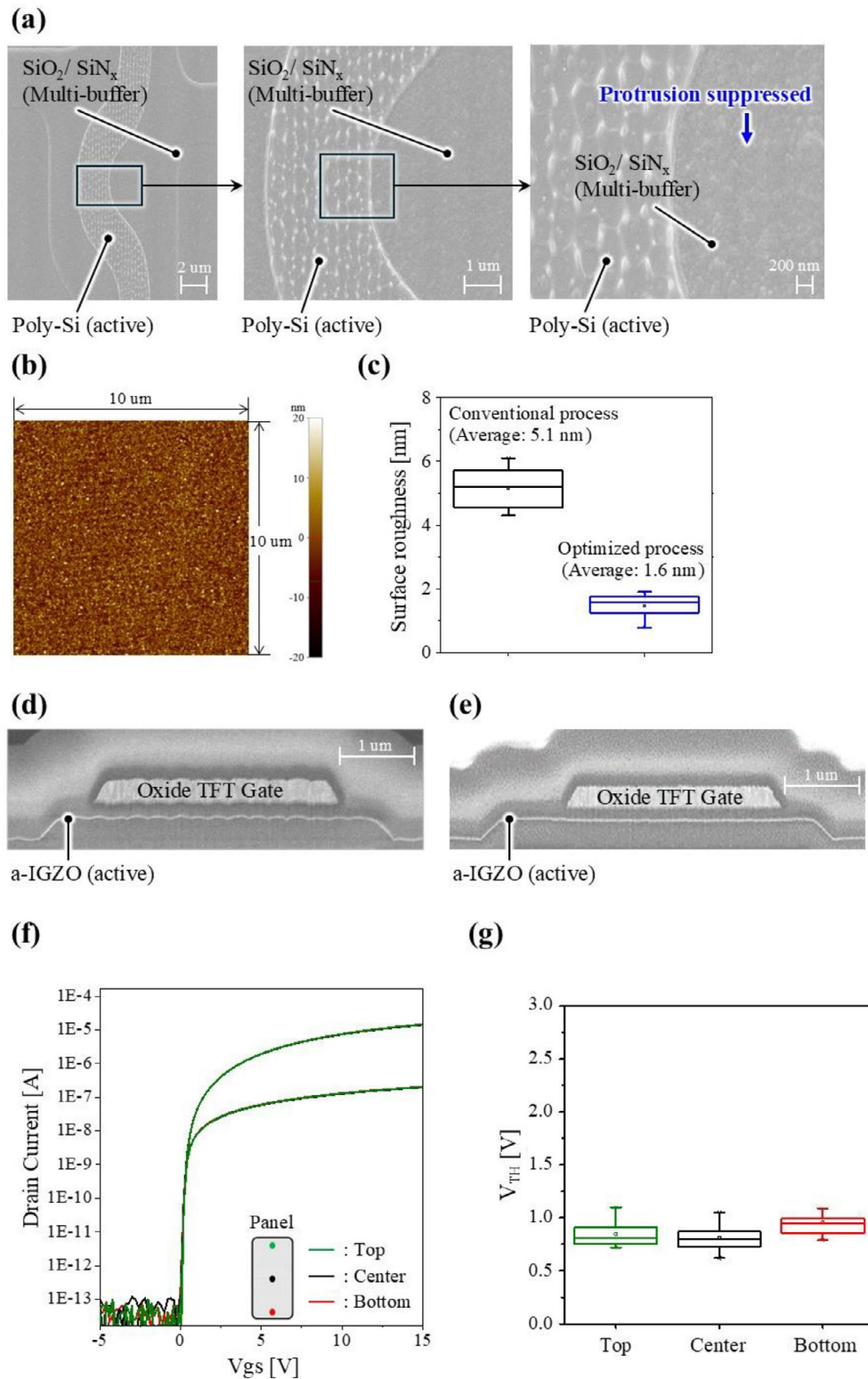


FIGURE 6 | Structural and electrical results obtained under the optimized LTPS active dry-etch condition. (a) SEM top-view images of the poly-Si active and multi-buffer layers after dry etching under the optimized DOE condition, showing a smooth interface with protrusions significantly suppressed. (b, c) AFM analysis results collected across multiple panels, demonstrating that the average surface roughness is reduced from 5.1 nm under the conventional process to 1.6 nm under the optimized process, confirming the suppression of multi-buffer protrusions. (d) FIB cross-sectional image of an oxide TFT fabricated under the conventional condition, showing noticeable protrusions transferred into the oxide channel. (e) FIB cross-sectional image of an oxide TFT fabricated under the optimized condition, exhibiting a uniform a-IGZO channel morphology without structural irregularities. (f) Electrical characteristics of oxide TFTs measured at the top (green), center (black), and bottom (red) regions of the panel after THB stress, showing highly consistent transfer curves. (g) Statistical distribution of V_{TH} values collected across multiple panels after THB stress, confirming that the optimized process improves within panel V_{TH} uniformity, reducing the variation from 0.92 to 0.15 V on average.

S1, key dry-etch parameters—including the etching gas, RF power, process time, and chamber pressure—were systematically varied to enhance etch selectivity without degrading the LTPS pattern. In the initial DOE, variations in RF power, process time, and chamber pressure while maintaining the original etching gas resulted in only limited improvement in poly-Si/SiO₂ etch selectivity. Therefore, an additional DOE focusing on the etching gas type was performed. With the modified etching gas, a clear enhancement in poly-Si/SiO₂ etch selectivity was achieved compared with the conventional condition. Among the evaluated DOE conditions, DOE3 exhibited the highest poly-Si/SiO₂ etch selectivity. This improvement in etch selectivity is directly reflected in the structural results. As shown in Figure S8, cross-sectional SEM images corresponding to the DOE conditions confirm that multi-buffer protrusion formation is effectively suppressed under the DOE3 condition. The optimized dry-etch condition (DOE3) was applied to panel fabrication. Figure 6 presents the structural and electrical improvements observed in oxide TFTs fabricated on panels processed under this optimized condition. The SEM top-view images in Figure 6a show that the multi-buffer layer exhibits a completely smooth surface without protrusions, clearly demonstrating an improvement compared with the conventional SEM top-view result shown in Figure 2c. The AFM measurements in Figure 6b,c further confirm this improvement, revealing that the surface roughness was significantly reduced from 5.1 nm under the conventional process to 1.6 nm after process optimization. As shown in Figure 6d, the conventional process resulted in noticeable surface protrusions, whereas the optimized condition in Figure 6e produced a uniform a-IGZO morphology without structural irregularities. The same improvement was reflected in device reliability. After THB testing, the transfer characteristics of oxide TFTs measured at the top (green), center (black), and bottom (red) regions of the panel, as shown in Figure 6f, exhibited highly consistent behavior with negligible variation. The statistical V_{TH} distribution in Figure 6g further confirms the improvement, showing that the V_{TH} variation across the panel, which had previously reached approximately 0.92 V within a single panel, was reduced to about 0.15 V under the optimized process. Moreover, reliability-induced defects observed in the conventional process were completely eliminated after applying the optimized condition. These results demonstrate that enhancing dry-etch selectivity during the LTPS TFT process effectively improved the stability of oxide TFTs in LTPO AMOLED displays.

3 | Conclusion

In this paper, we identified oxide TFT instability as the cause of image quality degradation in LTPO AMOLED displays after THB stress and proposed a process solution. Through structural and electrical analyses, we confirmed that oxide TFT instability occurs when the dry-etch selectivity between the poly-Si active and multi-buffer layers is insufficient, leading to a-IGZO channel protrusion variations within the panel. This a-IGZO channel protrusion variation causes differences in V_{TH} and mobility of the oxide TFT across different regions within the panel, ultimately resulting in image quality degradation under THB reliability stress. To address a-IGZO channel protrusion variations, the selectivity between the LTPS active layer and the multi-buffer layer must be improved. We conducted a DOE to optimize the

dry-etch process. Under the optimized conditions, the average protrusion height was reduced from 5.1 to 1.6 nm, significantly improving a-IGZO channel morphology uniformity and reducing the V_{TH} variation from approximately 0.9 to 0.15 V across multiple panels after THB stress. As a result, the oxide TFTs exhibited highly uniform electrical characteristics after reliability testing, and the horizontal line defects were completely eliminated. The results of this study demonstrate that differences in a-IGZO channel morphology lead to differences in oxide TFT device characteristics and affect display image quality. We believe that this research will improve the long-term reliability of displays using oxide TFTs and strengthen the foundation for next-generation mobile display technology.

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Supporting Information

Additional supporting information can be found online in the Supporting Information section.

Supporting File: aelm70424-sup-0001-SuppMat.docx.