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Research Article

Simultaneously Defined Semiconducting Channel Layer Using Electrohydrodynamic Jet Printing of a Passivation Layer for Oxide Thin-Film Transistors

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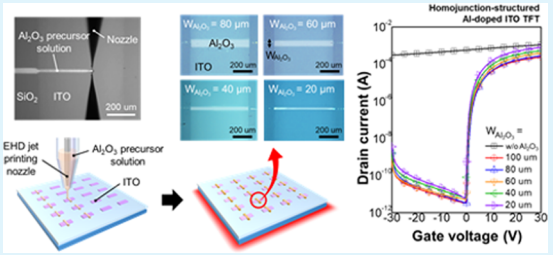
ABSTRACT: A simple fabrication method for homojunction-structured Al-doped indium−tin oxide (ITO) thin-film transistors (TFTs) using an electrohydrodynamic (EHD) jet-printed Al_2O_3 passivation layer with specific line ($W_{Al_2O_3}$) is proposed. After EHD jet printing, the specific region of the ITO film below the Al_2O_3 passivation layer changes from a conducting electrode to a semiconducting channel layer simultaneously upon the formation of the passivation layer during thermal annealing. The channel length of the fabricated TFTs is defined by $W_{Al_2O_3}$, which can be easily changed with varying EHD jet printing conditions, i.e., no need of replacing the mask for varying patterns. Accordingly, the drain current and resistance of the fabricated TFTs can be modified by varying the $W_{Al_2O_3}$. Using the proposed method, a transparent n-type metal−oxide−semiconductor (NMOS) inverter with an enhancement load can be fabricated; the effective resistance of load and drive TFTs is easily tuned by varying the processing conditions using this simple method. The fabricated NMOS inverter exhibits an output voltage gain of 7.13 with a supply voltage of 10 V. Thus, the proposed approach is promising as a low-cost and flexible manufacturing system for multi-item small-lot-sized production of Internet of Things devices.



KEYWORDS: *oxide thin-film transistor, solution process, electrohydrodynamic jet printing, passivation layer, diffusion*

1. INTRODUCTION

In the era of Internet of Things (IoT), a multitude of sensors, communication network technologies, and logic circuits have been developed.[1,2] As IoT technology continues to advance, the everyday connectivity of internet-enabled devices has become an increasingly important feature that requires low-power-consumption sensors and network systems.[3,4] In addition to the enhanced interconnection interface, the manufacturing system should possess the flexibility to satisfy customer needs in fast-changing industries. Therefore, a low-cost and flexible manufacturing system (FMS) for multi-item small-lot-sized production of IoT devices is required.[5−7]

Recently, oxide semiconductor-based thin-film transistors (TFTs) have become promising candidates for sensors, network systems, and logic circuit application because of their remarkable properties such as low leakage current, low subthreshold swing (SS), high field-effect mobility (μ_{FET}), good uniformity, and high transparency.[8] In particular, a low leakage current reduces power consumption. However, oxide TFTs are currently fabricated using subtractive manufacturing technology, i.e., photolithography.[9] Expensive photomasks are needed for this process, which involves multiple steps (photoresist deposition, exposure, development, etching, stripping, etc.) to form individual functional layers such as the gate, gate insulator, channel, and source/drain. Consequently, this technology is complex, costly, and inefficient; long fabrication times are required for prototype products, and to make changes to existing products.[10]

Here, a simple fabrication method for a homojunction-structured oxide TFT is suggested for a low-cost and FMS for IoT devices. Specifically, additive manufacturing technology using electrohydrodynamic (EHD) jet printing is applied, which has the advantages of low cost, a simple processing procedure, and no material waste. In addition, EHD jet printing produces a fine line width, such that device fabrication using this technology can accommodate high-resolution electronics for small-sized IoT devices with highly integrated circuits compared with most commonly used ink-jet printing.[11,12] The only procedure for the formation of the

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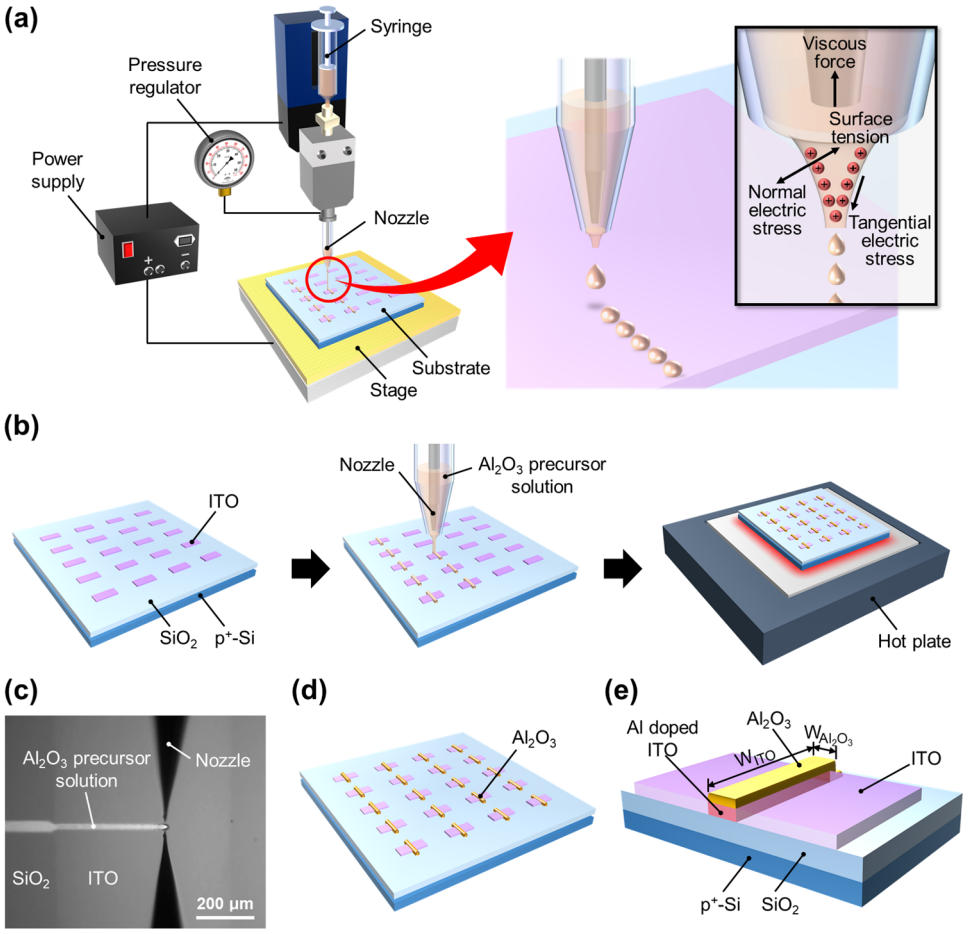

Figure 1. Schematic diagrams of the (a) EHD jet-printing system, and (b) fabrication process of homojunction-structured Al-doped ITO TFTs. (c) Photo image of EHD jet printing of Al_2O_3 precursor solution on the ITO film. (d) Schematic diagrams of the fabricated TFTs and (e) schematic structure of the fabricated TFT.

channel, source/drain, and passivation layer is printing of an Al_2O_3 precursor solution on top of an indium−tin oxide (ITO) line. After printing, this Al_2O_3 precursor solution is transformed into the passivation layer, and the specific area of ITO below the Al_2O_3 precursor solution forms an Al-doped ITO channel layer through a thermal annealing process. The line width of the printed Al_2O_3 precursor solution determines the feature size of the TFT, which can easily be modified by controlling the EHD jet-printing processing conditions; thus, the process offers flexibility. To demonstrate this simple method, we fabricated a transparent n-type metal−oxide−semiconductor (NMOS) inverter with an enhancement load. The resistance of load and drive TFTs in the NMOS inverter circuit was adjusted by varying the EHD jet-printing processing conditions of the Al_2O_3 passivation layer.

2. EXPERIMENTAL SECTION

2.1. TFT Fabrication. The homojunction-structured Al-doped ITO TFTs were fabricated with a bottom-gate structure. The ITO film was deposited using a radio frequency (RF) magnetron sputtering system via a shadow mask, to create a 4.83 nm layer on a heavily doped p-type Si wafer with a thermally oxidized 1200 Å thick SiO_2 film. The patterned ITO film had a W_{ITO} of 600 μm. The ITO target (diameter: 3 in.) consisted of In_2O_3/SnO_2 at a ratio of 9:1 (wt %). The power, deposition time, working pressure, and oxygen partial pressure ($[O_2]/[Ar + O_2]$) were fixed to 100 W, 2 min, 3.0 mTorr, and 40%, respectively. After electrode deposition, the samples were annealed in ambient air at 300 °C for 1 h. For the Al_2O_3 passivation layer, the Al_2O_3 precursor solution was prepared by dissolving 0.3 M aluminum nitrate nonahydrate ($Al(NO_3)_3{\cdot}9H_2O$, 98%; Sigma-Aldrich, St. Louis, MO) in 2-methoxyethanol. There were no additives to remove extra effect of other components. We used the lowest concentration at which printing uniformity was maintained, which was 0.3 M (Figure S1, Supporting Information).

The Al_2O_3 precursor solution, with a specific $W_{Al_2O_3}$ thickness, was printed on top of the ITO film using an EHD jet-printing system (eNano Jet Printer; ENJET, Gyeonggi-do, Korea). To control $W_{Al_2O_3}$ from 100 to 20 μm, the voltage applied between the nozzle tip and ground stage was varied from ±0.2 to ±0.4 kV, and the print speed was varied from 0.3 to 1.0 mm s^{-1} (Figure S2, Supporting Information). After printing, the samples were annealed in ambient air at 400 °C for 1 h. The W/L ratios of the fabricated TFTs were 600/100, 600/80, 600/60, 600/40, and 600/20 μm.

2.2. NMOS Inverter Fabrication. The transparent NMOS inverter with an enhancement load was fabricated with bottom-gate structured TFTs. A 200-nm-thick SiO_2 buffer layer was deposited onto a glass substrate using plasma-enhanced chemical vapor deposition (PECVD). An ITO gate electrode and SiO_2 gate insulator were deposited using an RF magnetron sputtering system and PECVD, respectively. After deposition of the buffer layer, gate, and gate insulator, the ITO film was deposited by RF magnetron sputtering via a shadow mask. In the patterned ITO film for the NMOS inverter with an enhancement load, the W_{ITO} of the load and drive TFTs were 500 and 2000 μm, respectively. The power, deposition time, working pressure, and $[O_2]/[Ar + O_2]$ were the same as those for a single homojunction-structured Al-doped ITO TFT. On top of the load and drive TFTs in the ITO film, an Al_2O_3 precursor

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solution was printed. After printing, thermal annealing at 400 °C was performed for 1 h. The W/L ratios of the load and drive TFTs were 500/300 and 2000/100 μm, respectively.

2.3. Device Characterization. The electrical characteristics of the TFTs and NMOS inverter were measured in a dark box in ambient air using a semiconductor parameter analyzer (HP 4156C; Agilent Technologies, Santa Clara, CA). Fabricated TFTs were examined using optical microscopy (OM). Cross-sectional images and EDS profiles of the ITO films were obtained by high-resolution transmission electron microscopy (HR-TEM) (JEM-ARM200F; JEOL Ltd., Tokyo, Japan). The composition of the ITO film was determined by time-of-flight secondary ion mass spectroscopy (TOF-SIMS) (TOF-SIMS 5; IONTOF GmbH, Münster, Germany). The chemical properties of the ITO film below the Al_2O_3 passivation layer were measured by X-ray photoelectron spectroscopy (XPS) (K-Alpha; Thermo Fisher Scientific, Waltham, MA).

3. RESULTS AND DISCUSSION

3.1. TFT Fabrication. Figure 1a shows the EHD jet-printing system used for fabrication of homojunction-structured Al-doped ITO TFTs. In this system, an Al_2O_3 precursor solution is supplied to a nozzle from a syringe and pulled to a fine tip. A high electric potential is then applied to the fluid to induce an electric field between the nozzle tip and ground stage.

Figure 1b shows the fabrication process for the Al-doped ITO TFTs. First, the ITO film was deposited, with a specific width, by radio frequency (RF) magnetron sputtering on a heavily doped p-type Si wafer with thermally oxidized SiO_2, via a shadow mask. Then, an Al_2O_3 precursor solution was printed, with a specific line width, on top of a specific area of the ITO film via EHD jet printing, as shown in Figure 1c and Video S1 (Supporting Information). Thermal annealing was conducted at 400 °C in air for 1 h. No semiconductor material deposition or patterning process was required with this procedure. The channel layer formed below the Al_2O_3 passivation layer simultaneously with the passivation layer formation after the thermal process. Figure 1d,e shows a schematic diagram of the fabricated device. Al_2O_3, Al-doped ITO, and the remaining ITO formed the passivation layer, channel, and source/drain, respectively. The widths of the ITO film (W_{ITO}) and printed Al_2O_3 passivation layer ($W_{Al_2O_3}$) define the channel width/length (W/L) ratio, i.e., W/L is defined by $W_{ITO}/W_{Al_2O_3}$. W_{ITO}, which determines W, follows the rectangular slot size of the shadow mask. $W_{Al_2O_3}$, which defines the L of the TFT, can be modified by varying the EHD printing process conditions, such as the electric field, printing speed, etc.[13]

3.2. Electrical Characteristics. Figure 2a shows the W/L ratio of homojunction-structured Al-doped ITO TFTs with various $W_{Al_2O_3}$ values. The Al_2O_3 precursor solution was printed on the ITO films, which had a fixed W_{ITO} of 600 μm and a $W_{Al_2O_3}$ that varied between 100 and 20 μm in 20 μm increments, i.e., the W/L ratios of the fabricated TFTs were 600/100, 600/80, 600/60, 600/40, and 600/20 μm, respectively. Figure 2b shows the evolution of the transfer characteristics of the fabricated TFTs as a function of $W_{Al_2O_3}$. The TFT without Al_2O_3 precursor solution printing showed no switching, as the bare ITO film essentially acted as a transparent conducting electrode with a high carrier concentration of over 10^{18} cm^{-3} (8.24×10^{19} cm^{-3} defined by Hall measurements).[14−17] However, TFTs with Al_2O_3 precursor solution printing showed proper switching. This indicates the

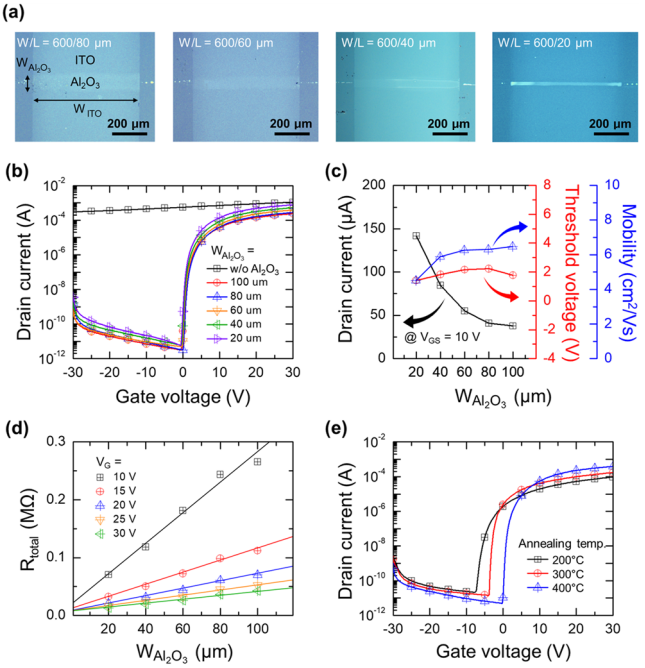

Figure 2. (a) OM images of the homojunction-structured Al-doped ITO TFT with varying $W_{Al_2O_3}$. (b) Transfer characteristics, (c) drain current at V_{GS} of 10 V, V_{th}, and μ_{FET}, and (d) R_{total} of the fabricated TFTs as a function of $W_{Al_2O_3}$. (e) Transfer characteristics of the fabricated TFTs as a function of annealing temperature.

formation of a semiconducting channel after Al_2O_3 precursor solution printing. In the case of the fabricated TFT with a W/L of 600/100 μm, μ_{FET}, threshold voltage (V_{th}), on/off current ratio, and SS were 6.46 ± 0.95 cm^2 V^{-1} s^{-1}, 1.78 ± 0.52 V, (7.47 ± 5.87) × 10^7, and 0.42 ± 0.03 V dec^{-1}, respectively (as shown Table 1). In addition, we summarized the statistical data of μ_{FET} and the V_{th} as shown in Figure S3 (Supporting Information). As can be seen in the data, the TFT device performances were also summarized in 10 samples and confirmed to be relatively uniform and repeatable.

Furthermore, the device showed little deviation in its hysteresis curve (Figure S4, Supporting Information). This indicates that the Al-doped ITO channel layer could be formed via an EHD jet-printed Al_2O_3 passivation layer without damage to the device.[18,19] Positive bias stress (PBS) and positive bias temperature stress (PBTS) tests were performed to evaluate device stability. The PBS test was performed for 10 000 s, with a gate voltage (V_{GS}) of 20 V and drain voltage (V_{DS}) of 10.1 V. The 1000 s PBTS test showed the following: V_{GS} = 20 V, V_{DS} = 10.1 V, and temperature equal to 50 °C.

After the PBS and PBTS tests, the associated V_{th} values of the device were 3.46 and 5.04 V, respectively (Figure S5, Supporting Information).

Moreover, the drain current increased as $W_{Al_2O_3}$ decreased, as shown in Figure 2c. This was attributed to a reduction in L of the homojunction-structured Al-doped ITO TFT.[20] However, the drain current was not inversely proportional to $W_{Al_2O_3}$. Comparing the fabricated TFT with $W_{Al_2O_3}$ values of 100 and 20 μm, the L of the TFT for which $W_{Al_2O_3}$ = 20 μm was one-fifth that of the TFT for which $W_{Al_2O_3}$ = 100 μm. Unlike the rate of change in L, the drain current of the TFT for which $W_{Al_2O_3}$ = 20 μm was 3.7-fold that of the TFT for which $W_{Al_2O_3}$ =

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Table 1. Extracted Parameters of the Homojunction-Structured Al-Doped ITO TFT with Various $W_{ITO}/W_{Al_2O_3}$

$W_{ITO}/W_{Al_2O_3}$ (μm)	μ_{FET} ($cm^2\ V^{-1}\ s^{-1}$)	V_{th} (V)	on/off current ratio	SS ($V\ dec^{-1}$)
600/100	6.46 ± 0.95	1.78 ± 0.52	(7.47 ± 5.87) × 10^7	0.42 ± 0.03
600/80	6.29 ± 1.13	2.23 ± 0.28	(8.63 ± 3.22) × 10^7	0.42 ± 0.02
600/60	6.25 ± 0.89	2.17 ± 0.35	(7.93 ± 4.88) × 10^7	0.42 ± 0.03
600/40	5.87 ± 0.88	1.83 ± 0.51	(8.76 ± 3.52) × 10^7	0.42 ± 0.03
600/20	3.74 ± 0.97	1.41 ± 0.42	(1.11 ± 3.84) × 10^8	0.41 ± 0.04

100 μm. This is to be expected given that the relative influence of the resistance of the source (R_S) and resistance of the drain (R_D) with respect to the total resistance (R_{total}) increases as L decreases.[3,21] Due to this, the μ_{FET} of the TFT for which $W_{Al_2O_3}$ = 20 μm was underestimated, as 3.74 $cm^2\ V^{-1}\ s^{-1}$, compared with that for which $W_{Al_2O_3}$ = 100 μm. Figure 2d shows the R_{total} for various $W_{Al_2O_3}$ values as a function of the applied V_{GS}. The R_{total} of homojunction-structured Al-doped ITO TFTs at V_{GS} = 10 V decreased from 0.27 to 0.07 $\mu\Omega$ with decreasing $W_{Al_2O_3}$, from 100 to 20 μm. This trend is also attributable to the influence of R_S and R_D.

The homojunction-structured Al-doped ITO TFTs annealed at temperatures below 400 °C exhibited a negative shift in V_{th}, as shown in Figure 2e. This is likely due to insufficient diffusion of Al ions into the ITO film from the Al_2O_3 passivation layer. Furthermore, the devices annealed at 200 and 300 °C showed a reduced on-current compared with those annealed at 400 °C. This resulted from a remaining NO_3^- ion-coordinated effect arising from the Al_2O_3 precursor solution, which could act as trap sites in the ITO film and an interface between the ITO film and Al_2O_3 passivation layer.[22,23] Thus, an annealing temperature of 400 °C was necessary to obtain the desired switching characteristics.

3.3. Physical and Chemical Analyses. Time-of-flight secondary ion mass spectroscopy (TOF-SIMS) was used to examine Al ion diffusion into the ITO film in the region below the Al_2O_3 passivation layer. Figure 3a,b show the depth of Al ion diffusion in the TFT annealed at 200 and 400 °C, respectively. In the TFT annealed at 200 °C, the depth of Al ion diffusion was about half the thickness of the ITO film. This indicates that the thermal energy associated with an annealing temperature of 200 °C was insufficient for Al ion diffusion from the Al_2O_3 passivation layer to the bottom of the ITO film. However, the Al ion diffused more deeply into the ITO film in the TFT annealed at 400 °C, as shown in Figure 3c, i.e., near the ITO/SiO_2 interface.

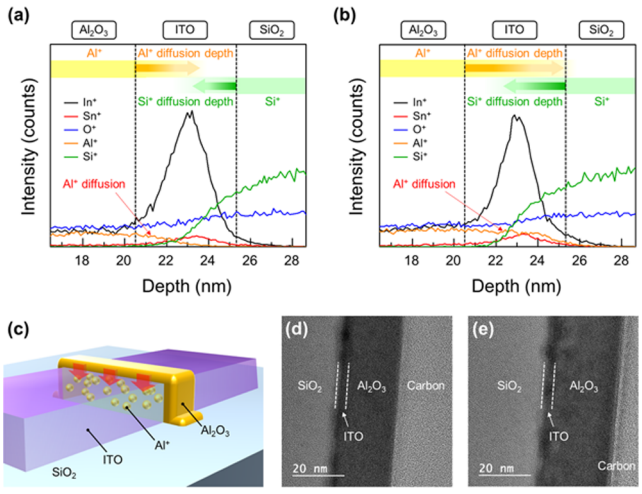

Figure 3. TOF-SIMS depth profiles of the homojunction-structured Al-doped ITO TFTs annealed at (a) 200 °C and (b) 400 °C. (c) Schematic diagram of the diffusion of Al ions from the Al_2O_3 passivation layer annealed at 400 °C. Cross-sectional HR-TEM images of the fabricated TFTs annealed at (d) 200 °C and (e) 400 °C.

Diffusion of Si ions from the SiO_2 gate insulator was also confirmed. However, the Si ions did not fully diffuse throughout the entire depth of the ITO film, even at 400 °C. Therefore, it is evident that the diffusion depth of the Al ion originating from the Al_2O_3 passivation layer affects the electrical characteristics of the ITO film beneath this passivation layer.

Cross-sectional high-resolution transmission electron microscopy (HR-TEM) was also used to confirm the diffusion of Al ions from the Al_2O_3 passivation layer. Figure 3d,e shows a dark-field HR-TEM image of Al-doped ITO TFTs annealed at 200 and 400 °C, respectively. Compared with the TFT annealed at 200 °C, the Al_2O_3/ITO interface formed an intermixed layer; it was difficult to detect the Al_2O_3/ITO interface of the TFT annealed at 400 °C.

Energy-dispersive spectroscopy (EDS) scanning of the TFT annealed at 400 °C was conducted to measure the distribution of the diffused Al ions, and a gradient distribution of Al atoms from the Al_2O_3/ITO interface to the bottom of the ITO film was confirmed (Figure S6, Supporting Information).

It has been reported that Si and Al ions can act as oxygen binders and reduce oxygen vacancies (V_O) in oxide films.[14] While Ga is commonly used as a carrier suppressor in indium–zinc oxide (IZO) and ITO, these metal (i.e., Si and Al) atoms are promising alternatives for Ga.[14,24,25] This may be due to the low standard electrode potential (SEP) of Si (−1.697 V) and Al (−1.66 V), which strengthen the metal oxide bond more effectively than Ga (SEP: −0.52 V) in oxide films.[26−28]

Previously, the role of Si ions diffused from the gate insulator, as a carrier suppressing the dopant in indium–zinc oxide, was verified by our group.[29] Likewise, the diffused Si ions in the ITO film likely modulate the carrier concentration of ITO. However, the diffusion length of a Si ion is not sufficiently long to suppress the carrier concentration over the entire ITO film. In contrast, Al ions could affect the whole ITO film, given that Al ions diffused into the ITO/SiO_2 interface from the top surface of the ITO film, i.e., the Al_2O_3 passivation layer. Therefore, diffusion of Al ions from the Al_2O_3 passivation layer could compensate for the parts of the ITO film at which the carrier concentration is insufficiently suppressed by Si ion diffusion from the SiO_2 gate insulator. Thus, the whole ITO film can be modulated by dual diffusion of Si and Al ions originating from a SiO_2 gate insulator and Al_2O_3 passivation layer, respectively, as shown in Figure 4a.

X-ray photoelectron spectroscopy (XPS) depth analysis of the ITO film was performed to demonstrate the effect of the

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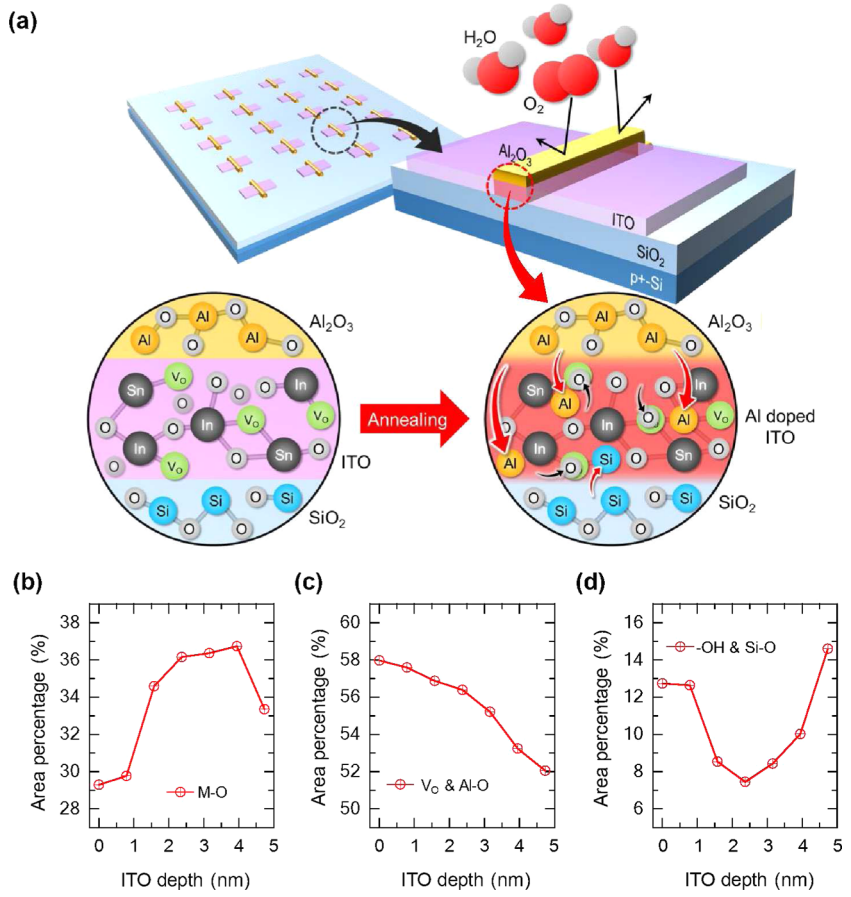

Figure 4. (a) Schematic showing the mechanism for semiconducting channel layer formation in the ITO film below the Al_2O_3 passivation layer. Area percentages of (b) M−O, (c) V_O and Al−O, and (d) −OH and Si−O as a function of depth of the ITO film.

diffused Si and Al ions in the homojunction-structured Al-doped ITO TFT. The O 1s spectra of the ITO film were measured in seven steps from Al_2O_3/ITO to the ITO/SiO_2 interface. Each O 1s spectrum was deconvoluted into three peaks centered at 530.1 ± 0.2 (O_I), 531.0 ± 0.2 (O_{II}), and 532.0 ± 0.2 eV (O_{III}); these features correspond to the In and Sn metal oxide bond (M−O), V_O and Al−O (V_O and Al−O), and metal hydroxide species −OH and Si−O (−OH and Si−O), respectively.[30−33] Figure 4b−d shows the area ratio of M−O, V_O and Al−O, and −OH and Si−O spectra in O 1s XPS depth spectra of the ITO film with respect to the Al_2O_3/ITO interface (at 0 nm) and the ITO/SiO_2 interface (at 4.83 nm). In Figure 4b, the variation in area ratio for M−O shows a concave downward curve with respect to the depth from the Al_2O_3/ITO and ITO/SiO_2 interfaces. This corresponds to a gradual reduction in the ratio of In−O and Sn−O due to the diffusion of Al ions from the Al_2O_3/ITO interface and Si ions from the ITO/SiO_2 interface. The area ratios for M−O are relatively low near Al_2O_3/ITO and ITO/SiO_2 due to the presence of Al−O and Si−O. Since the diffusion depth of the Si ion is shallower than that of the Al ion, the highest area ratio for M−O is situated toward the ITO/SiO_2 interface. Figure 4c shows a gradual decrease in the area ratio of V_O and Al−O, which is mainly due to the concentration distribution of diffused Al ions from the Al_2O_3 passivation layer. The variation in the area ratio of −OH and Si−O shows a convex downward curve with depth from the Al_2O_3/ITO interface to the ITO/SiO_2 interface, as shown in Figure 4d. It is difficult to determine the bond responsible for this feature, as −OH and Si−O have similar binding energies. However, the area ratio of −OH and Si−O near the ITO/SiO_2 interface can be attributed to the diffusion of Si ions from the SiO_2 gate insulator, based on the TOF-SIMS results. In contrast, the area ratio of −OH and Si−O near the Al_2O_3/ITO interface is attributable to solution processing of the Al_2O_3 passivation layer. Consequently, diffusion of Al ions from the Al_2O_3 passivation layer and Si ions from the SiO_2 gate insulator was confirmed; thus, the electrical characteristics of the ITO film were modulated through the formation of Al−O and Si−O.

3.4. Application to Electronic Circuit: Transparent NMOS Inverter. To demonstrate the potential of the proposed fabrication method for circuit fabrication and applications, a fully transparent NMOS inverter was fabricated, as shown in Figure 5a.[34] The proposed inverter was fabricated with a bottom-gate structure on a glass substrate. First, the glass substrates with SiO_2 buffer, an ITO gate electrode, and a SiO_2 gate insulator layer were prepared. Then the ITO film for the NMOS inverter with an enhancement load was deposited by RF magnetron sputtering via a shadow mask. The W_{ITO} of the patterned ITO film for the load TFT was 500 μm and that for a drive TFT was 2000 μm. After ITO deposition, the Al_2O_3 precursor solution was printed with a specific $W_{Al_2O_3}$ value via EHD jet printing on top of a specific region of the ITO film. Finally, thermal annealing was conducted at 400 °C in air for 1 h. To modulate the effective resistance of each TFT, the Al_2O_3 passivation layers for the load and drive TFTs were printed with $W_{Al_2O_3}$ values of 300 and 100 μm, respectively. Here, the

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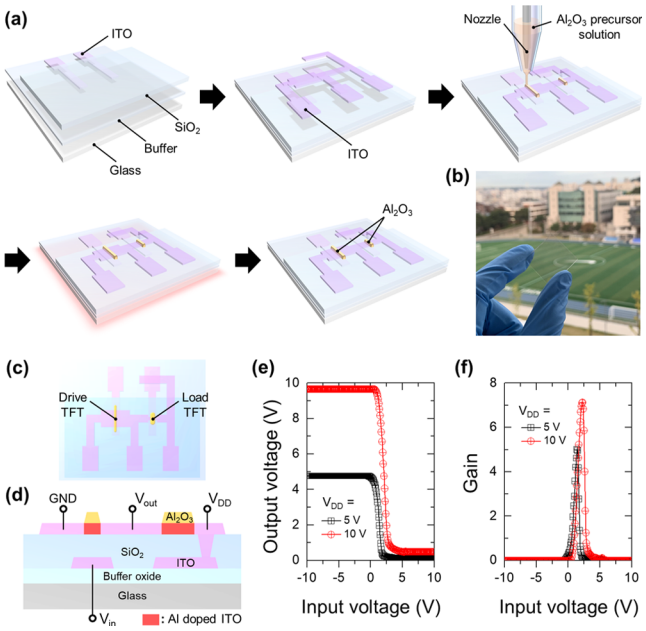

Figure 5. (a) Schematic diagrams of the fabrication process of the transparent NMOS inverter with enhancement mode load. (b) Photo image, (c) schematic top view and (d) cross-sectional view of the fabricated inverter. (e) Voltage transfer curve and (f) output voltage gain of the fabricated inverter.

deposition and patterning of the semiconductor material were not conducted in our fabrication procedure; the only process required to create the load and drive TFTs was Al_2O_3 precursor solution printing. As shown in Figure 5b, the fabricated NMOS inverter was transparent. Figure 5c,d shows schematic diagrams of the fabricated device. The $W_{ITO}/W_{Al_2O_3}$ ratio for the load and drive TFTs was 500/300 and 2000/100 μm, respectively, i.e., $(W/L)_{load}$ = 500/300 μm and $(W/L)_{drive}$ = 2000/100 μm; the β ratio ($(W/L)_{drive}/(W/L)_{load}$) was 12. Figure 5e shows the voltage transfer curve of the NMOS inverter at supply voltages (V_{DD}) of 5 and 10 V. The output high and low voltages were 4.76 and 0.12 V for a V_{DD} of 5 V, and 9.65 and 0.48 V for a V_{DD} of 10 V, respectively. The high output voltage did not reach the V_{DD} value because the load TFT always operates in the saturation region when using an inverter with an enhancement load.[35,36] At the inversion voltage, output voltage gains of 5.00 and 7.13 were determined for V_{DD} at 5 and 10 V, respectively (as shown in Figure 5f).

4. CONCLUSIONS

Here, a simple method for fabricating homojunction-structured Al-doped ITO TFTs was proposed. Using EHD jet printing, an Al_2O_3 precursor solution was printed onto a specific area of the ITO film. After thermal annealing, the specific region of the ITO film below the Al_2O_3 passivation layer changed from a conducting electrode to a semiconducting channel layer simultaneously with the passivation layer formation. The semiconductor material deposition and patterning processes were omitted from this TFT fabrication procedure. The formation of the semiconducting channel layer was mainly attributed to the diffusion of Al ions from the Al_2O_3 passivation layer during the thermal annealing process. Because the $W_{Al_2O_3}$ of the printed Al_2O_3 precursor solution defines the W/L ratio of the fabricated TFT, the electrical characteristics of the device can be modified by varying EHD jet-printing processing conditions. The fabricated TFT with a W/L ratio of 600/100 μm exhibited a μ_{FET} of 6.46 $cm^2\ V^{-1}\ s^{-1}$, V_{th} of 1.78 V, and a drain current of 37.64 μA at a V_{GS} of 10 V. Meanwhile, the drain current increased to 141.89 μA (3.7-fold) at a V_{GS} of 10 V when the $W_{Al_2O_3}$ of the printed Al_2O_3 passivation layer was 20 μm, i.e., W/L of 600/20 μm. Furthermore, the transparent NMOS inverter was fabricated using this simple method. The W/L ratios of the load and drive TFTs were also controlled by EHD jet-printing conditions for the Al_2O_3 passivation layer. The output voltage gain of the NMOS inverter was 7.13 with a W/L ratio of 500/300 μm for the load TFT and 2000/100 μm for the drive TFT. Thus, this simple method for fabricating homojunction-structured TFTs using an EHD jet-printed Al_2O_3 passivation layer is promising as a low-cost and FMS for multi-item small-lot-sized production of IoT devices (Figure S7, and associated text, Supporting Information).

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.0c07091.

ITO film was deposited, with a specific width, by radio frequency (RF) magnetron sputtering on a heavily doped p-type Si wafer with thermally oxidized SiO_2, via a shadow mask. Then, an Al_2O_3 precursor solution was printed, with a specific line width, on top of a specific area of the ITO film via EHD jet printing (AVI)

Line width results of optical microscope analysis according to various printing condition; statistical data; hysteresis characteristic of homojunction-structured Al-doped ITO TFT; EDS scan profile of homojunction-structured Al-doped ITO TFT annealed at 400 °C; (a) the OM image of minimum line width of Al_2O_3 ink using an ink-jet printing system and (b) transfer characteristics of the Al-doped ITO TFT (PDF)

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Notes

The authors declare no competing financial interest.

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